TAN-19

Application Note – Considerations for Designing the XRT7250 and XRT7300 Device in a DS3 Line Card Application (Preliminary)

Rev. 1.00

April 7, 2000

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1.0 INTRODUCTION

The purpose of this document is to provide the reader with knowledge of the considerations that must be employed when designing the both XRT7250 DS3/E3 Framer IC and the XRT7300 DS3/E3/STS-1 LIU IC into a DS3 Line Card Application design.

This document will provide the user with the following guidelines for designing with these two products.

a. Bellcore System requirement guidelines
b. Hardware Design guidelines

c. Software Design guidelines

1.1 A BRIEF DESCRIPTION OF THE XRT7300 DS3/E3/STS-1 LIU IC

The XRT7300 DS3/E3/STS-1 LIU IC is a single-chip Line Interface Unit that is capable of supporting data transmission at the following data rates:

- DS3 – 44.736MHz
- E3 – 34.368MHz
- STS-1 – 51.84MHz

Figure 1 presents an illustration of a Functional Block Diagram of the XRT7300 DS3/E3/STS-1 LIU IC.

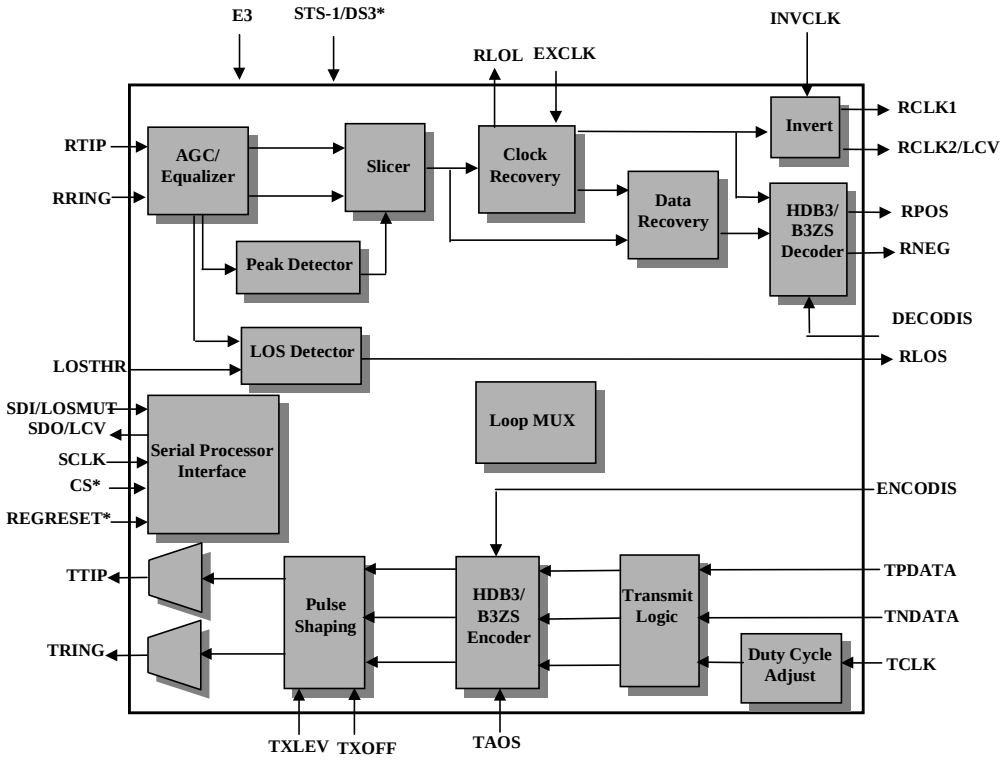

Figure 1, Illustration of the Function Block Diagram of the XRT7300 DS3/E3/STS-1 LIU IC.

The Functional Blocks, within the XRT7300 LIU IC are briefly discussed below.

The Transmit Section

In the Transmit Direction, the XRT7300 device was specifically design to accept either TTL or CMOS level signal from the local Terminal Equipment (e.g., the XRT7250 Framer, in this case) and convert it into a pulse that complies with either of the following "Isolated Pulse Template" requirements.

- Bellcore GR-499-CORE (for DS3 Applications)
- ITU-T G.703 (for E3 Applications)
- Bellcore GR-253-CORE (for STS-1 Applications)

Figure 1 indicates that the Transmit Section consists of the following functional blocks.

- The "Transmit Clock Duty Cycle Adjust" PLL
- The "Transmit Logic" Block
- The "HDB3/B3ZS" Encoder
- The "Transmit Pulse Shaping" Block

Each of the "Transmit Section" Functional Blocks are briefly discussed below.

The "Transmit Clock Duty Cycle Adjust PLL" Block

The "Transmit Pulse Shaping" Block (within the XRT7300 LIU IC) requires a line rate clock signal, with a duty cycle of 50% in order to generate pulses that are compliant with the various "Pulse Template Requirements". Rather than forcing the user to condition and apply a 44.736MHz clock signal (which happens to have a duty cycle or 50%), the "Transmit Clock Duty Cycle Adjust PLL" block accepts the TCLK signal (from the "Framer IC") and synthesizes a "line rate" clock signal, which has a duty cycle of 50%. The "Transmit Clock Duty Cycle Adjust PLL" permits the user to apply a line rate signal (at the "TCLK" input pin) with a duty cycle ranging between 30 and 70%. This functional block alleviates the user of the burden and the cost of having to include a clock driver on the board (for the sole purpose of cleaning up the duty cycle of this signal).

The "Transmit Logic" Block

The "Transmit Logic" block is responsible for latching the data, on the "TPDATA" and "TNDATA" input pins (via the appropriate edge of the TCLK signal), and making this "latched" data available to the remainder of the "Transmit Section" within the XRT7300 LIU IC.

The "Transmit Logic" block will (by default) latch the contents of the "TPDATA" and "TNDATA" signals upon the falling edge of "TCLK". However, if the XRT7300 device is operating in the "Host" Mode, then the user can configure the "Transmit Logic" block

to sample "TPDATA" and "TNDATA" upon the rising edge of "TCLK" by writing a "1" into bit D2 (TxCLKINV) within Command Register CR1; as illustrated below.

			Register Bit-Format				
Address	**Command Register**	**Type**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	RO	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	TXOFF	TAOS	TXCLKINV 1	TXLEV	TXBIN
0x02	CR2	R/W	DECODIS	ENCODIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	RNRZ	LOSMUT	RCLK2/ LCV*	RCLK2INV	RCLK1INV
0x04	CR4	R/W	Reserved	STS-1/ DS3*	E3	LLB	RLB
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x08	CR8	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

The Transmit Logic Block can also be configured to accept data (from the Framer IC) in the "Single-Rail" format. This can be accomplished via either of the following two means.

1. Tying the "TNDATA" input pin to "GND" and applying all of the "outbound" DS3 data stream to the "TPDATA" input pin via a binary data stream.

NOTE: The user must also apply a line rate (44.736MHz) clock signal to the TCLK input pin. The "outbound" DS3 data stream (being applied to the "TPDATA" input pin) must be aligned with this 44.736MHz clock signal.

2. Configuring the "Transmit Section" (within the LIU IC) to accept "Single-Rail" data. If the XRT7300 device is operating in the "Host" Mode, then this is accomplished by writing a "1" into the "TxBIN" bit-field (within Command Register CR1); as illustrated below.

			Register Bit-Format				
Address	**Command Register**	**Type**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	RO	RLOL	RLOS	ALOS	DLOS	DMO
0x01	CR1	R/W	TXOFF	TAOS	TXCLKINV	TXLEV	TXBIN 1
0x02	CR2	R/W	DECODIS	ENCODIS	ALOSDIS	DLOSDIS	REQDIS
0x03	CR3	R/W	RNRZ	LOSMUT	RCLK2/ LCV*	RCLK2INV	RCLK1INV
0x04	CR4	R/W	Reserved	STS-1/ DS3*	E3	LLB	RLB
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x08	CR8	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

By executing this step, the "Transmit Section" of the XRT7300 device will be configured to only accept and latch data via the "TPDATA" and "TNDATA" input pins. Further, the XRT7300 device will also be configured to ignore any data applied to the "TNDATA" input pin.

CAUTIONARY NOTE ABOUT OPERATING THE TRANSMIT SECTION (OF THE XRT7300 DEVICE) IN THE "SINGLE-RAIL" MODE

It is imperative that the user enable the "B3ZS/HDB3" Encoder (within the LIU IC) anytime the "Transmit Section" has been configured to operate in the "Single-Rail" Mode.

The "HDB3/B3ZS" Encoder Block

This block (if enabled) will encode the "outbound" data into the HDB3 format (for E3 applications) or the B3ZS format (for DS3 and STS-1 applications). This functional block can be enabled or disabled by pulling the "ENCODIS" input pin "LOW" or "HIGH", respectively..

The "Transmit Pulse Shaping" Block

This function block is responsible for generating bipolar pulses that comply with the various "Pulse Template Requirements". The "Transmit Pulse Shaping" block also includes a "Line Build-Out" Circuit which can be enabled or disabled for DS3 and STS-1 applications.

NOTES:
1. The "Transmit Line Build-Out" circuit is automatically disabled if the XRT7300 is operating in the "E3" Mode.
2. The "Transmit Line Build-Out" circuitry (within the Transmit Pulse Shaping Block) can be enabled or disabled by pulling the "TxLEV" input pin "LOW" or "HIGH", respectively.

The Receive Section

In the Receive Direction, the XRT7300 device was designed to receive a line signal, which has been distorted by cable loss, and perform clock and data recovery on this data. The XRT7300 device will then output this clock and data to the local Terminal Equipment, via CMOS level signals.

Figure 1 indicates that the Receive Section consists of the following functional blocks.

- The "AGC/Equalizer" Block
- The "Peak Detector" and "Slicer" block
- The "Clock and Data Recovery" block
- The "HDB3/B3ZS Decoder" block

Each of the "Receive Section" Functional Blocks are briefly discussed below.

The "AGC/Equalizer" Block

This functional actually consists of two sub-blocks.

- The AGC (Automatic Gain Control) Block
- The "Equalizer" block

The purpose of the AGC block is to accommodate any "flat" (or "resistive") loss that the DS3 line signal will incur as it travels from the Remote Terminal Equipment to the "Receive Inputs" of the XRT7300 device. This sub-block is very helpful in those system applications that have been designed for redundancy. This is due to the fact that a common approach to system redundancy design is to include a "cable-splitter" in the "Receive Path". This permits the "Receive" Line signal to be routed to both a "Primary" and "Back-up" line card, in parallel. This "cable-splitter" typically imposes a flat loss of about 6dB.

The purpose of the Equalizer block is to accommodate "cable" (or "frequency-dependent") loss.

The "Peak Detector" and "Slicer" block
The purpose of this functional block is to accept an amplified and equalized line signal, and quantify each symbol as being either a "1" or a "0".

The "Clock and Data Recovery" block
The purpose of this functional block is to extract both data and timing information from the "received line signal". This timing information is output to the Framer IC via the "RCLK1" and "RCLK2" output pins. The recovered data is output (to the Framer) via the "RPOS" and "RNEG" output pins. The "RCLK1" or "RCLK2" output signals are ultimately used by the "Receive Section" of the Framer IC, in order to latch the "incoming" E3 or DS3 data stream.

The "HDB3/B3ZS Decoder" block
This block (if enabled) will decode the "incoming" data from the "HDB3 format" (for E3 applications) or the B3ZS format (for DS3 and STS-1 applications). This functional block can be enabled or disabled by pulling the "DECODIS" input pin "LOW" or "HIGH", respectively.

NOTE: For a detailed and complete description of the XRT7300 DS3/E3/STS-1 LIU IC, please consult the "XRT7300 DS3/E3/STS-1 LIU IC" Data Sheet.

1.2 A BRIEF DESCRIPTION OF THE XRT7250 DS3/E3 FRAMER IC

The XRT7250 DS3/E3 Framer IC is a single-chip device that is capable of supporting data transmission at the following data rates:

- DS3 – 44.736MHz
- E3 – 34.368 MHz

Figure 2 presents a Functional Block Diagram of the XRT7250 DS3/E3 Framer IC.

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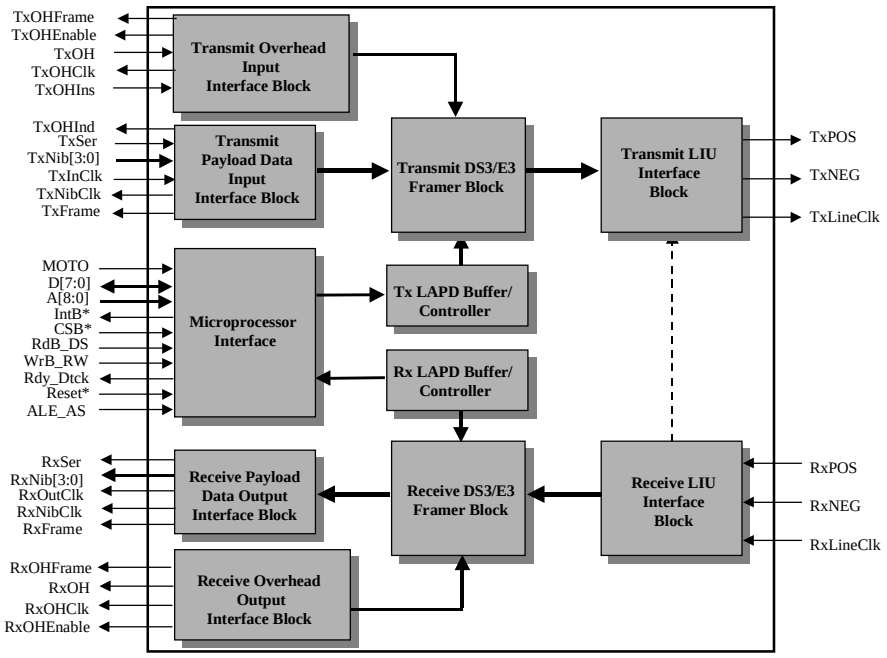


Figure 2, An Illustration of the Functional Block Diagram of the XRT7250 DS3/E3 Framer IC

According to Figure 2, the XRT7250 DS3/E3 Framer IC consists of the following functional blocks.

- The Transmit Payload Data Input Interface block
- The Transmit Overhead Data Input Interface block
- The Transmit HDLC Controller Block
- The Transmit DS3/E3 Framer Block
- The Transmit LIU Interface Block
- The Microprocessor Interface block
- The Receive LIU Interface Block
- The Receive DS3/E3 Framer Block
- The Receive HDLC Controller Block
- The Receive Payload Data Output Interface block
- The Receive Overhead Data Output Interface block

The role/function of each of these Functional Blocks is briefly described below.

1.2.1 Operation of the "Transmit Payload Data Input Interface" block

The purpose of the "Transmit Payload Data Input Interface" block is to accept the user data from the Terminal Equipment. The XRT7250 Framer IC will then take this user data and insert it into the payload bit-fields, within the "outbound" DS3 frames.

NOTE: The XRT7250 Framer IC can be configured to accept the user data (from the Terminal Equipment) in either a "serial" or "nibble-parallel" manner.

1.2.2 Operation of the "Transmit Overhead Data Input Interface" block

By default, the "Transmit Section" of the XRT7250 Framer IC will internally generate and insert the overhead bits into each "outbound DS3" frame. However, the "Transmit Overhead Data Input Interface" block permits the user's external data link layer equipment to insert its own overhead bits into the "outbound DS3" frames. These externally inserted overhead bits will over-write the internally generated overhead bits.

The XRT7250 Framer IC offers two different methods for "inserting" these overhead bits into the "outbound" DS3 frames. Each of these methods are presented in Section _.

1.2.3 The Transmit HDLC Controller Block

The purpose of the "Transmit HDLC Controller" block is two-fold.

1. To support the processing of "outbound" LAP-D Message frames carrying PMDL (Path Maintenance Data Link) messages; and
2. To support the processing of "outbound" FEAC (Far-End Alarm & Control) Messages.

1.2.4 The Transmit DS3/E3 Framer Block

The purpose of the "Transmit DS3/E3 Framer" block is to accept data from the following sources, and generate a constant stream of consecutive "outbound" DS3 or E3 frames.

- The Transmit Payload Data Input Interface Block
- The Transmit Overhead Data Input Interface Block
- The Transmit HDLC Controller Block
- Internally generated Overhead bits

This DS3 or E3 data stream will then be routed to the "Transmit LIU Interface" block for further processing.

1.2.5 The Transmit LIU Interface Block

The purpose of the "Transmit LIU Interface" block is two-fold.

1. To receive "outbound" DS3/E3 data (from the Transmit DS3/E3 Framer block) and to optionally encode the "outbound" DS3/E3 data stream into either the B3ZS or HDB3 format, and
2. To transmit this "outbound" (and perhaps encoded) DS3/E3 data stream (and clock signal) to the LIU IC, via either the "Single-Rail" or "Dual-Rail" mode.

1.2.6 The Microprocessor Interface Block

The purpose of the Microprocessor Interface block is two-fold.

1. To permit the Microprocessor/Microcontroller to configure the XRT7250 Framer IC into the desired mode of operation; and
2. To permit the Microprocessor/Microcontroller to enable and service "XRT7250 Framer" related interrupts.
3. To permit the Microprocessor/Microcontroller to write the contents of an "outbound" PMDL message into the "Transmit LAPD Message" buffer.
4. To permit the user to read in the contents of a "newly" received PMDL message.

1.2.7 The Receive LIU Interface Block

The purpose of the "Receive LIU Interface" block is two-fold.

1. To receive an "inbound" (and perhaps encoded) DS3/E3 data stream from the LIU IC, via either the "Single-Rail" or "Dual-Rail" mode.
2. To optionally decode this "inbound" DS3/E3 data from either the B3ZS or HDB3 format, back into a binary data stream.

NOTE: If the "B3ZS/HDB3 Decoder" (within the Framer IC) is enabled, then the "Receive LIU Interface block is responsible for detecting and declaring Line Code Violations (LCVs).

1.2.8 The Receive DS3/E3 Framer Block

The purpose of the "Receive DS3/E3 Framer" block is to receive the "inbound" DS3 or E3 data, from the "Receive LIU Interface" block, and to do the following with this data.

1. To Acquire and Maintain Frame Synchronization with the "inbound" DS3 or E3 frames.
2. To route the contents of all "payload" bits (within the inbound DS3 or E3 frames) to the "Receive Payload Data Output Interface" block.
3. To route the contents of all "overhead" bits (within the inbound DS3 or E3 frames) to the "Receive Overhead Data Output Interface" block.
4. To route the contents of all "DL" and "FEAC" bits (for DS3 applications), "N" bits (for E3/ITU-T G.751 applications) and "GC" or "NR" bytes (for E3/ITU-T G.832 applications) to the Receive HDLC Controller block.

5. To Declare and Clear all of the following alarm condition: AIS, OOF, LOS, and FERF.
6. To detect the occurrence of "P" bit errors, "CP" bit errors, FEBE events (for DS3 applications), BIP-8 errors, FEBE events (for E3, ITU-T G.832 applications) and BIP-4 errors (for E3, ITU-T G.751 applications).

1.2.9 The Receive HDLC Controller Block

The purpose of the "Receive HDLC Controller" block is two-fold.

1. To support the processing of "inbound" LAP-D Message frames carrying PMDL messages, and
2. To support the processing of "inbound" FEAC (Far-End Alarm & Control) Messages.

1.2.10 Operation of the "Receive Payload Data Output Interface" block

The purpose of the "Receive Payload Data Output Interface" block is to output the user (service) data (of the "inbound" DS3 frames) to the Terminal Equipment.

NOTE: The XRT7250 Framer IC can be configured to output user to (to the local Terminal Equipment) in either a "serial" or "nibble-parallel" manner.

1.2.11 Operation of the "Receive Overhead Data Output Interface" block

The purpose of the "Receive Overhead Data Output Interface" block is to output the overhead bits (of the "inbound" DS3 frames) to the external data link equipment.

NOTE: For a more detailed and complete discussion of each of these functional blocks within the XRT7250 Framer IC, please consult the "XRT7250 DS3/E3 Framer IC" Data Sheet.

2 A BRIEF SUMMARY OF DS3 REQUIREMENTS

2.1 DS3 LIU REQUIREMENTS

An LIU IC, which has been designed for DS3 applications, is required to meet numerous "Transmit" and "Receive" Physical Layer requirements. Some of these requirements may or may not be applicable to a given system application. Whenever any of these requirements are "universally" applicable to all DS3 applications, this document will indicate so. The following sections will discuss each of these requirements in detail.

2.1.1 LIU RECEIVER REQUIREMENTS

For most DS3 applications, the LIU IC has the following requirements imposed on it.

- Receive Sensitivity Requirements.
- Jitter Tolerance Requirements
- Jitter Transfer Requirements (applicable to "Transport Equipment" applications)

Each of these LIU Receiver Requirements are briefly summarized below.

2.1.1.1 LIU RECEIVE SENSITIVITY REQUIREMENTS

The Use of the Receive Equalizer in a Typical DS3 or STS-1 Application

Most System Manufacturers (of equipment supporting DS3 and STS-1 lines) will interface their equipment to a DSX-3 or STSX-1 Cross-Connect equipment.

NOTE: The "DSX-3" and "STSX-1" Cross Connect equipment should not be confused with a "Digital Cross Connect System" (DCS). The "DSX-3" or "STSX-1" is typically an electromechanical piece of equipment which is very similar to a patch-panel. The "DSX-3" is the location where pulse template measurements and verification are made.

While installing their equipment, the "Transmit Line Build-Out" circuit will be set to the proper setting, such that the transmit output pulse is compliant with the "Isolated DSX-3, or STSX-1 Pulse Template" requirements. (Recall that for the XRT7300 device, this is achieved by setting the "TxLEV" input pin or bit-field to the appropriate level).

When the System Manufacturer is interfacing the Receive Section of the XRT7300 device to the DSX-3 Cross Connect system, he/she is aware of the following facts.

- By definition, all DS3 or STS-1 line signals that are present at the Cross Connect (DSX-3 or STSX-1) location are required to meet the "Isolated Pulse Template Requirements" (per Bellcore GR-499-CORE for DS3 applications, or Bellcore GR-253-CORE for STS-1 applications).

- Further, these Bellcore documents state that the amplitude of these pulses (at the DSX-3 or STSX-1 location) can range in amplitude from 360mVpk to 850mVpk.

- Finally, these Bellcore documents stipulate that the Receiving Terminal must be able to receive this "pulse-template" compliant line signal over a cable length of 0 to 450 feet from the DSX-3 or STSX-1 location.

These facts are also reflected below in Figure 3.

NOTE: The LIU Receive Sensitivity requirements are applicable to all DS3 Line Cards that were intended to transmit and receive DS3 line signals over coaxial cable.

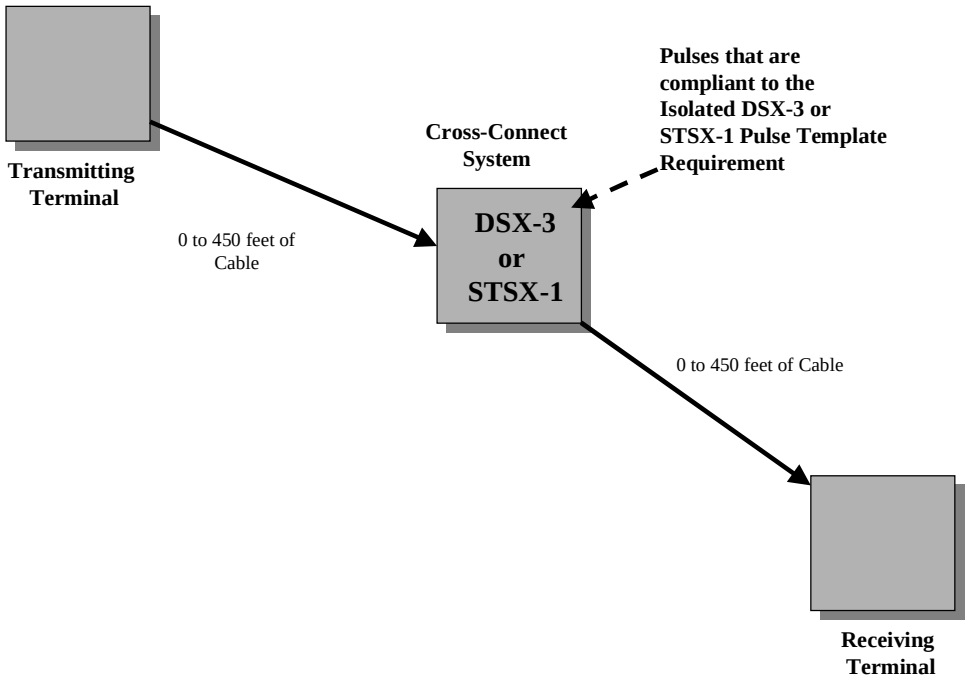


Figure 3, Illustration of the Typical Application for the System Installer.

Design Considerations (for DS3 and STS-1 Applications)

When installing equipment into environments as depicted in Figure 3, we recommend that the user enable the Receive Equalizer (within the XRT7300 LIU device) for all cable lengths between the RTIP/RRING input pins of the XRT7300 device and the "DSX-3" location. This can be accomplished by setting the REQDIS input pin or bit-field to "0". In fact, the only time that the user should disable the Receive Equalizer is when an off-chip equalizer in the Receive path, between the DSX-3 location and the RTIP/RRING input pins, or in applications where the Receiver is monitoring the transmit output signal of the "Local Terminal Equipment" directly.

2.1.1.2 JITTER TOLERANCE REQUIREMENTS – PER BELLCORE GR-499-CORE

The various Bellcore and ANSI specification documents require that a given DS3 terminal be capable of "tolerating a certain of amount of jitter" in the "incoming" line signal. In other words, the DS3 Terminal Equipment must be able to receive a DS3 line signal (which contains a certain amount of jitter), in an un-erred manner.

Bellcore GR-499-CORE, when specifying this jitter tolerance requirements, categorizes "DS3 Terminal Equipment" Interfaces into two categories.

Category I Type of Equipment
Interfaces for signals that the equipment asynchronously multiplexes into, or de-multiplexes from, higher rate signals.
Example of Category I Equipment:

- Most low speed interfaces to multiplexes,
- Add/Drop Multiplexers (ADMs), and
- Digital Cross-Connect Systems (DCSs).

Category II Type of Equipment
Category II – Interfaces for signals for which the equipment does one of the following:

a. Regenerates
b. Demultiplexes into, or creates by multiplexes from, lower rate signals.
c. Synchronously multiplexes into, or demultiplexes from, higher-rate signals.

Examples of Category II Equipment:

- Interfaces for the high speed interfaces to multiplexes, ADMs, and DCSs,
- Digital terminal interfaces of a Digital Loop Carrier (DLC) system,
- Repeater interfaces.

The "Jitter Tolerance" requirements (per Bellcore GR-499-CORE) for "Category I and II" type of equipment is presented below.

2.1.1.2.1 Bellcore GR-499-CORE Jitter Tolerance Requirements for Category I type of Equipment.

The Jitter Tolerance requirements (per Bellcore GR-499-CORE) is expressed as a function of "Maximum Tolerable" jitter vs "Jitter Frequency". The Jitter Tolerance requirements for "Category I Type of Equipment" is presented below in Figure _.

Figure _, An Illustration of the Jitter Tolerance Requirements for Category I Type of Equipment (per Bellcore GR-499-CORE).

2.1.1.2.2 Bellcore GR-499-CORE Jitter Tolerance Requirements for Category II type of Equipment

To be included in the next revision of this document

2.1.1.3 JITTER TRANSFER REQUIREMENTS – PER BELLCORE GR-499-CORE

To be included in the next revision of this document

2.1.1.4 ABSOLUTE MAXIMUM JITTER REQUIREMENTS – PER BELLCORE GR-499-CORE

To be included in the next revision of this document

2.1.2 LIU TRANSMIT REQUIREMENTS

2.1.2.1 ISOLATED PULSE TEMPLATE REQUIREMENTS

In most DS3 applications, the Transmit Output of the DS3 Line Card is going to be routed to a Cross Connect System (aka., the DSX-3), over coaxial cable.

NOTE: The "DSX-3" is typically an "Electromechanical" system (similar to a "patch-panel") that functions as a "central connection" point for each system (with a DS3 Line Card) in the "room".

According to Bellcore GR-499-CORE, this Cross Connect System can reside anywhere from 0 to 450 feet from the "Transmit Output" of the DS3 Line Card. This same Bellcore document also indicates that if this line signal is terminated at the Digital Cross Connect system, this line signal must meet the following requirements.

a. The amplitude of each pulse (within the line signal) must range between 350mVpk and 850mVpk.
b. The shape of each pulse (when plot on an oscilloscope) must reside entirely within the "Upper" and "Lower" Curves, as depicted in Figure 4.

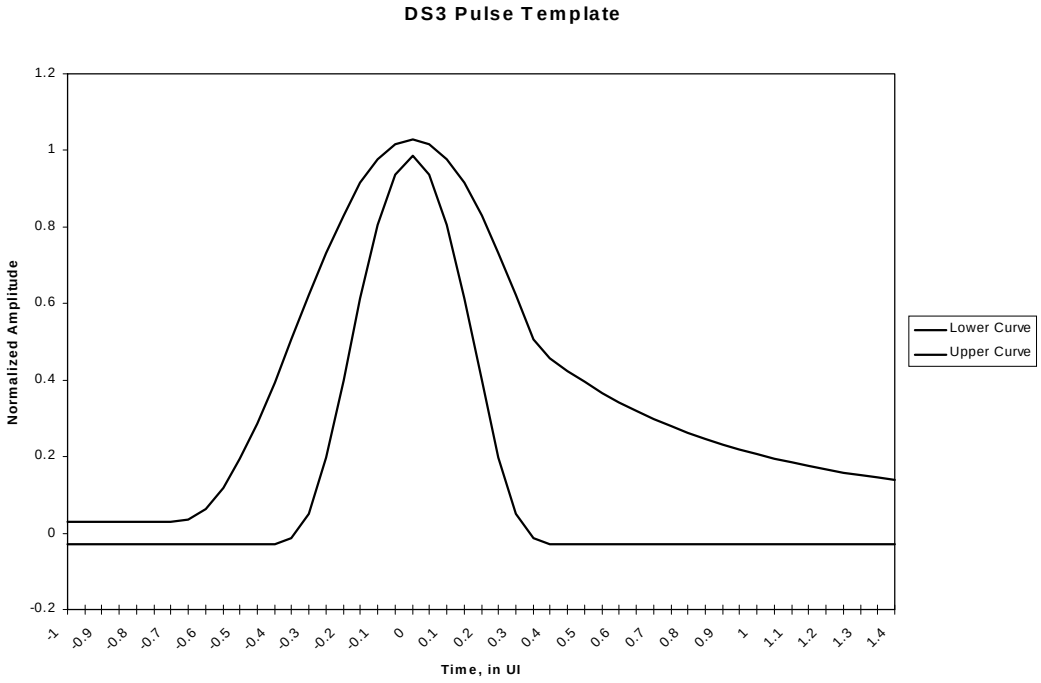


Figure 4, Illustration of the "Isolated Pulse Template Requirements" per Bellcore GR-499-CORE (for DS3 applications)

The XRT7300 DS3/E3/STS-1 LIU was specifically designed to meet this particular "Isolated Pulse Template Requirement" (for DS3 applications).

2.1.2.2 ENABLING/DISABLING THE TRANSMIT LINE BUILD-OUT, DURING SYSTEM INSTALLATION

For DS3 Line Card applications, it is imperative that the system designer permit the "Transmit Line Build-Out" circuit to be "field selectable" (e.g., either be enabled or disabled, upon system installation).

When a system is being installed, the DS3 line cards (within the system) will be electronically connected to the DSX-3 Cross Connect system. However, during the installation process, a check is typically done in order to insure that the transmit output

pulse of the DS3 line card meets the "Isolated Pulse Template requirement – per Bellcore GR-499-CORE" (when measured at the DSX-3 location).

As mentioned earlier, the transmit output of the DS3 line card is required to meet this "Isolated Pulse Template requirement" over all cable lengths, ranging from 0 to 450 of cable. For DS3 applications (e.g., data rates at 44.736MHz), meeting this can be a very difficult task, for the following reasons.

- A given transmitter that is capable of generating pulses that comply with the "Isolated Pulse Template", when the cable length (between the Transmitting Terminal and the DSX-3) is 450 feet, will not be able to meet the "Isolated Pulse Template", when the cable length is 0 feet. (e.g., the pulses will be too "square-shaped" at short cable lengths).
- A given transmitter that is capable of generating pulses that comply with the "Isolated Pulse Template", when the cable length is 0 feet, will not be able to meet the "Isolated Pulse Template" at 450 feet. (e.g., the pulses will be too distorted at longer cable lengths).

As a consequence, the XRT7300 device contains a "Line Build-Out" circuit which either "shapes" or does not "shape" the pulses within the "outbound" DS3 line signal. The "Line Build-Out" circuit is controlled by the "TxLEV" input pin of the XRT7300 device.

Setting the "TxLEV" input pin to "GND", enables the "Line Build-Out" circuit, within the XRT7300 device. In this mode, the XRT7300 device will automatically "pre-shape" pulses (within the "outbound" DS3 line signal) prior to transmission onto the line. These pulses will be "pre-shaped" such that they will comply with the "Isolated Pulse Template" requirements for DS3 applications, over short cable lengths (e.g., less than 225 feet).

Conversely, setting the "TxLEV" input pin to "VDD", disables the "Line Build-Out" circuit, within the XRT7300 device. In this mode, the XRT7300 device will NOT "pre-shaped" pulses (within the "outbound" DS3 line signal) prior to transmission onto the line. These pulses will (in general) be "square" in shaped, and will not comply with the "Isolated Pulse Template" requirements for DS3 applications, over short cable lengths. However, as these pulses travel over longer lengths of cable, then cable loss (e.g., frequency-dependent loss) will cause the pulses to become "shaped" and ultimately comply with the "Isolated Pulse Template" requirements, over longer cable lengths (e.g., greater than 225 feet).

Application Note – Considerations for Designing the XRT7250 and XRT7300 Device in a DS3 Line Card Application (Preliminary)

Rev. 1.00

April 7, 2000

THE "RULE OF THUMB" FOR ENABLING/DISABLING THE TRANSMIT LINE BUILD-OUT WITHIN THE XRT7300 LIU IC.

1. The user is advised to enable the "Transmit Line Build-Out" circuit (e.g., pull the "TxLEV" pin to "GND", if the cable length between the Transmitting Terminal and the Digital Cross-Connect System (DSX-3) is less than 225 feet.
2. The user is advised to disable the "Transmit Line Build-Out" circuit (e.g., pull the "TxLEV" pin to "VDD", if the cable length between the Transmitting Terminal and the Digital Cross-Connect System (DSX-3) is greater than 225 feet.

TYPICAL APPROACH TO ENABLING/DISABLING THE TRANSMIT LINE BUILD-OUT CIRCUIT (WITHIN THE LIU IC) DURING SYSTEM INSTALLATION

The typical procedure for choosing to enable or disable the Transmit Line Build-out circuit (within the LIU IC) is as follows.

a. Electrically connect the "Transmitting Terminal" to the "DSX-3" via coaxial cable. However, in this case, the cable (as the DSX-3 end) should be terminated at 75 ohms.
b. Configure the Framer IC to transmit a series of "isolated" pulses (e.g., each "pulse" typically separated by at least four (4) zeros).

NOTE: In order to accomplish this, the user will typically have to disable the "B3ZS" encoders within both the LIU and the Framer IC.

c. Capture these "isolated" pulses on a ____ scope (or newer model), and check to see if the pulses comply with the "Pulse Template" requirements.
d. If the pulses comply, then leave the "TxLEV" input pin (on the XRT7300 device) in its current state.
e. If the pulses do not comply with the "Pulse Template" requirements, then toggle the state of the "TxLEV" input pin (of the XRT7300 device) and then repeat procedure (c). In this case, the transmit output pulse (of the XRT7300 device) should now meet the "Isolated Pulse Template" requirements.

2.2 DS3 FRAMER REQUIREMENTS

2.2.1 THE DS3 FRAMING STRUCTURE

The role of the various overhead bits are best described by discussing the DS3 Frame Format as a whole. The DS3 Frame contains 4760 bits, of which 56 bits are overhead and the remaining 4704 bits are "payload" bits. The "payload" data is formatted into packets of 84 bits and the overhead (OH) bits are inserted between these payload packets. The XRT7250 Framer device supports the following two DS3 framing formats:

- C-bit Parity
- M13

Figures 5 and 6 present the DS3 Frame Format for C-bit Parity and M13, respectively.

X	I	F1	I	AIC	I	F0	I	NA	I	F0	I	FEAC	I	F1	I
X	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I
P	I	F1	I	CP	I	F0	I	CP	I	F0	I	CP	I	F1	I
P	I	F1	I	FEBE	I	F0	I	FEBE	I	F0	I	FEBE	I	F1	I
M0	I	F1	I	DL	I	F0	I	DL	I	F0	I	DL	I	F1	I
M1	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I
M0	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I

X = Signaling bit for network control
I = Payload Information (84 bit packets)
Fi = frame synchronization bit with logic value i
P = parity bit
Mi = multiframe synchronization bit with logic value i
AIC = application identification channel
NA = reserved for network application
FEAC = far end alarm and Control
DL = data link
CP = C-bit parity
FEBE = far end block error
UDL = User Data Link

Figure 5, DS3 Frame Format for C-bit Parity

X	I	F1	I	C11	I	F0	I	C12	I	F0	I	C13	I	F1	I
X	I	F1	I	C21	I	F0	I	C22	I	F0	I	C23	I	F1	I
P	I	F1	I	C31	I	F0	I	C32	I	F0	I	C33	I	F1	I
P	I	F1	I	C41	I	F0	I	C42	I	F0	I	C43	I	F1	I
M0	I	F1	I	C51	I	F0	I	C52	I	F0	I	C53	I	F1	I
M1	I	F1	I	C61	I	F0	I	C62	I	F0	I	C63	I	F1	I
M0	I	F1	I	C71	I	F0	I	C72	I	F0	I	C73	I	F1	I

X = Signaling bit for network control
I = Payload Information (84 bit packets)
Fi = frame synchronization bit with logic value i
Cij = jth stuff code bit of ith channel
P = parity bit
Mi = multiframe synchronization bit with logic values i

Figure 6, DS3 Frame Format for M13

2.2.2 THE DEFINITION, USE AND HANDLING OF THE DS3 OVERHEAD BITS

2.2.2.1 THE P-BITS

The “Transmit DS3 Framer” block (within the XRT7250 Framer IC) computes the “even-parity” value of the contents of a given DS3 frame. The resulting parity value is inserted into the two “P” bit-fields, within the very next “outbound” DS3 frame.

The “Receive DS3 Framer” block (at the remote terminal equipment) will verify the value of the “P-bits” as it receives these DS3 frames. If the “Receive DS3 Framer” block, (within the XRT7250 device) receives a given DS3 frame, with the correct “P-bit” values, then it will presume that it has received this particular DS3 frame, in an “error-free” manner. Conversely, if the “Receive DS3 Framer” block receives a given DS3

frame, with the incorrect "P-bit" values, then it will presume that it has received this particular DS3 frame, in an "erred" manner.

If the "Receive DS3 Framer" block (within the XRT7250 Framer IC) detects a "P-Bit" Error, then it will do the following.

- ***Generate the "Detection of P-Bit Error" Interrupt.***
  - In doing this, the XRT7250 device will assert the "active-low" Interrupt Request" output pin by driving it "LOW".
  - Additionally, the XRT7250 device will assert the "P-Bit Error Interrupt Status" bit-field, within the "RxDS3 Interrupt Status Register" as depicted below.

RxDS3 Interrupt Status Register (Address = 0x13)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	1

- ***Increment the "PMON Parity Error Count" Registers, as indicated below.***

PMON Parity Error Count Register - MSB (Address = 0x54)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Parity Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON Parity Error Count Register - LSB (Address = 0x55)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Parity Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

2.2.2.2 THE CP-BITS

The role of the "CP" bit is very similar to that of the "P" bit, except for the following.

1. CP-bits are used to permit performance monitoring over an entire DS3 path (e.g., from the "Source" Terminal Equipment; through any number of "mid-network" terminals to the "Sink" Terminal Equipment).
2. P-bits are used to permit performance monitoring of a DS3 data stream, as it is transmitted from one Terminal Equipment to an adjacent Terminal Equipment.

How CP-bits are Processed

The following sections describe how the CP-bits are processed at three locations.

- The "Source" Terminal Equipment
- The "Mid-Network" Terminal Equipment
- The "Sink" Terminal Equipment

Figure _ presents a simple illustration of the location of these three types of Terminal Equipment, within the Wide-Area-Network.

Application Note – Considerations for Designing the XRT7250 and XRT7300 Device in a DS3 Line Card Application (Preliminary)

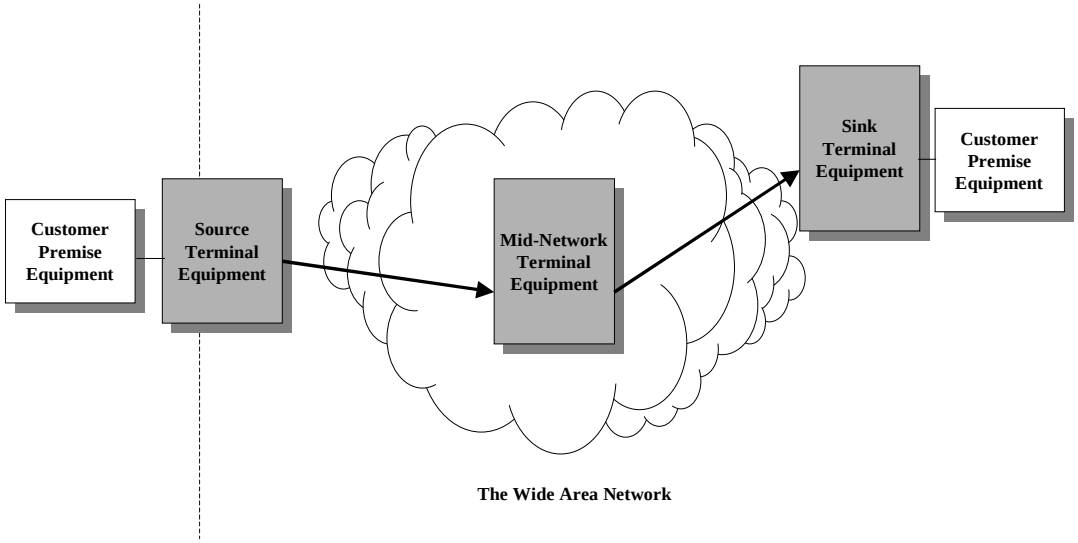


Figure _, A Simple Illustration of the location of the "Source", Mid-Network" and "Sink" Terminal Equipment (for CP-bit Processing)

NOTE: The use of the terms "Source" and "Sink" Terminal Equipment are employed to simplify this discussion of "CP-Bit Processing". In reality, the "Source" Terminal Equipment (in Figure _) will also function as the "Sink" Terminal Equipment (for DS3 traffic traveling in the opposite direction). Likewise, the "Sink" Terminal Equipment (in Figure _) will also function as the "Source" Terminal Equipment.

CP-Bit Processing at the "Source" Terminal Equipment

The "Source" Terminal Equipment (located at one edge of the WAN) will typically receive its DS3 payload data from some Customer Premise Equipment (CPE). As the "Source" Terminal Equipment receives this data from the CPE, it will compute the even-parity value over all bits within a given "outbound" DS3 frame. The Terminal Equipment will then insert this even parity value into both of the P-bit fields and both of the CP-bit fields, within the very next "outbound" DS3 frame.

Hence, both the P-bit values and the CP bit values will originate at the "Source" Terminal Equipment.

CP-Bit Processing at the "Mid-Network" Terminal Equipment

The "Mid-Network" Terminal Equipment has the task of doing the following.

- Receiving a DS3 data stream, via the "Receive WAN Interface" Line Card.
- Transmitting this same DS3 data stream (out to another Remote Terminal Equipment) via the "Transmit WAN Interface" Line Card.

Figure _ presents an illustration of the basic architecture of the "Mid-Network" Terminal Equipment.

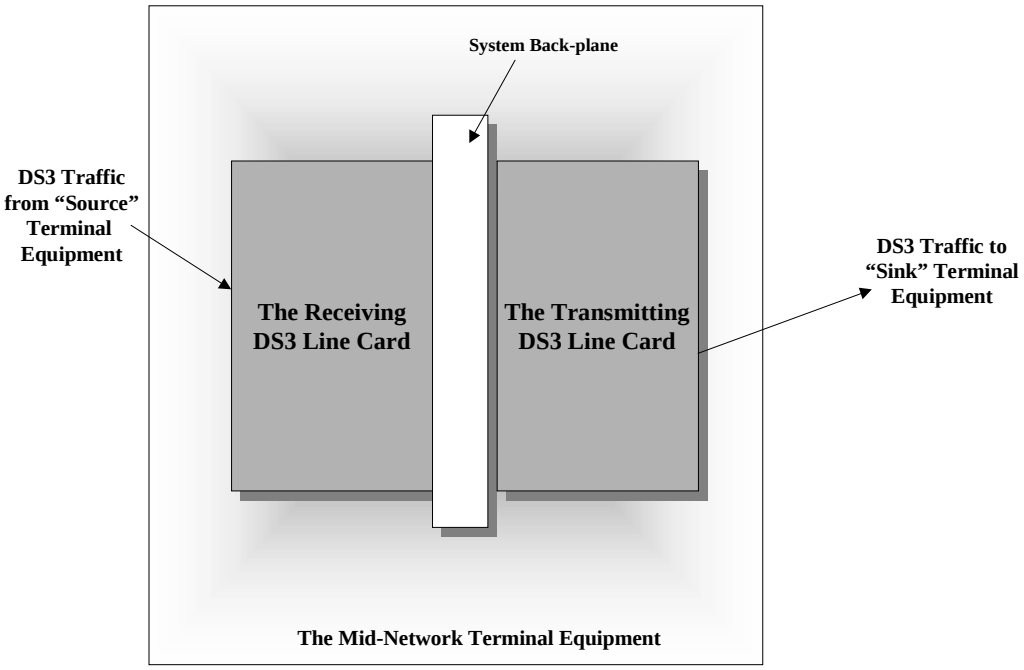


Figure _, Illustration of the Presumed Configuration of the "Mid-Network" Terminal Equipment.

Operation of the Receive WAN Interface Line Card

The "Receive WAN Interface" Line Card receives a DS3 data stream from a "Remote Terminal Equipment". As the "Receive WAN Interface" Line Card does this, it will also do the following.

1. Compute and verify the P-bits of each "inbound" DS3 frame.
2. Compute and verify the CP-bits are each "inbound" DS3 frame.
3. Output both the "payload" and "overhead" bits to the system back-plane.

Operation of the "Transmit WAN Interface" Line Card.

The "Transmit WAN Interface" Line Card receives the "outbound" DS3 data stream from the "Receive WAN Interface" Line Card (via the System Back-Plane). As the "Transmit WAN Interface" Line Card receives this data, it will also do the following.

1. Extract out the "CP-bit" values, from the "Receive WAN Interface" Line Card (via the System Back-Plane) and insert these values into the CP-bit fields, within the "outbound" DS3 data stream; via the Transmit Overhead Data Input Interface" block of the XRT7250 Framer IC.
2. Compute the even-parity over all bits, within a given "outbound" DS3 frame, and insert this value into the "P-bits" within the very next "outbound" DS3 frame.
3. Transmit this resulting DS3 data stream to the "Remote Terminal Equipment".

Processing at the "Sink" Terminal Equipment

The "Sink" Terminal Equipment (located at the opposite edge of the Wide-Area-Network, from the "Source" Terminal Equipment) will receive and transmit this DS3 data stream. As the "Sink" Terminal Equipment receives this DS3 data stream, it will also do the following.

1. Compute and verify the "P-bits" within each "inbound" DS3 frame.
2. Compute and verify the "CP-bits" within each "inbound" DS3 frame.

WHAT IMPACT DOES THIS HAVE ON YOUR DS3 LINE CARD DESIGN?

In some system applications, the user will have to include some glue logic, in order to support CP-bit processing. Whether this glue logic is necessary depends upon whether your system is located at the "Edge of the Network" or in the "Middle of the Network".

If your DS3 Line Card exists in "Edge of the Network" type equipment.

If the DS3 Line Card is intended for an "Edge of the Network" type system (e.g., where the DS3 data stream is both sourced and terminated), then the XRT7250 Framer IC will "take care" of everything.

In the "Transmit Direction" the Transmit DS3 Framer block will (by design) compute the even parity of a given DS3 frame and then insert this parity results into both the "P" bits and the "CP" bits within the very next "outbound" DS3 frame.

In the "Receive Direction" the Receive DS3 Framer block will compute and verify both the "P" and "CP" bits, within each "inbound" DS3 frame. If the "Receive DS3 Framer" block (within the XRT7250 Framer IC) detects a "CP-Bit" Error, then it will do the following:

- ***Generate the "Detection of CP-Bit Error" Interrupt.***
  - In doing this, the XRT7250 device will assert the "active-low" Interrupt Request" output pin by driving it "LOW".
  - Additionally, the XRT7250 device will assert the "CP-Bit Error Interrupt Status" bit-field, within the "RxDS3 Interrupt Status Register" as depicted below.

RxDS3 Interrupt Status Register (Address = 0x13)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CP-Bit Error Interrupt Status	LOS Interrupt Status	AIS Interrupt Status	Idle Interrupt Status	FERF Interrupt Status	AIC Interrupt Status	OOF Interrupt Status	P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
1	0	0	0	0	0	0	0

- Increment the "PMON CP-Bit Error Count" Registers, as indicated below.

PMON CP-Bit Error Count Register - MSB (Address = 0x58)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CP Bit Error Count - High Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

PMON CP-Bit Error Count Register - LSB (Address = 0x59)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CP Bit Error Count - Low Byte							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

If your DS3 Line Card exists in the "Middle of the Network" type equipment

If the DS3 Line Card is intended for a "Middle of the Network" type system (e.g., where the DS3 data stream is received (via one port) and is transmitted (via another port), then the user must include the necessary glue-logic in order to do the following.

- To extract out the value of the "CP" bit, within each "incoming" DS3 frame; and
- To insert this value into the "CP" bit-field within this same DS3 frame, as it is transmitted out of the "Terminal Equipment".

2.2.2 The FEAC (Far-End Alarm and Control) Bit-field

Each DS3 frame consists of 1 FEAC bit-field. The purpose of this FEAC bit-field is to transmit "Bit-Oriented Signaling" (BOS) from one Terminal Equipment to another. The following sections describe the following.

- The meaning behind the FEAC bit-fields
- How the XRT7250 Framer IC supports the transmission and reception of these FEAC Messages.

2.2.2.1 TRANSMITTING AND RECEIVING FEAC (FAR-END ALARM & CONTROL) MESSAGES

If the XRT7250 Framer IC is configured to operate with the DS3/C-Bit Parity Framing format, then it can be configured to transmit "FEAC" Messages.

FEAC (Far-End-Alarm & Control) is a standard "Bit-Oriented Signaling" method that is defined by Bellcore GR-499-CORE. These "FEAC Messages" are transmitted via the "FEAC" bit-field within each outbound DS3 frame, as illustrated below.

X	I	F1	I	AIC	I	F0	I	NA	I	F0	I	FEAC	I	F1	I
X	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I
P	I	F1	I	CP	I	F0	I	CP	I	F0	I	CP	I	F1	I
P	I	F1	I	FEBE	I	F0	I	FEBE	I	F0	I	FEBE	I	F1	I
M0	I	F1	I	DL	I	F0	I	DL	I	F0	I	DL	I	F1	I
M1	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I
M0	I	F1	I	UDL	I	F0	I	UDL	I	F0	I	UDL	I	F1	I

Figure 7, Illustration of the DS3 Framing Format (C-Bit Parity), with the "FEAC" bit-field highlighted.

Figure 7 indicates that each DS3 frame consists of only one FEAC bit-field.

The actual message, that is to be sent (via these FEAC Messages) consists of six (6) bits. As a consequence, there are 64 possible FEAC Message values that can be transmitted to the remote terminal equipment. Of these 64 values, 43 values have been defined in Bellcore GR-499-CORE, to have some meaning. Table 1 presents the relationship between these FEAC code words, and their Meaning.

Table 1, The Relationship between the FEAC six-bit Code Words and their Meaning

FEAC Code Word	Meaning	Comments
011001	DS3 Equipment Failure – Service Effecting	The Terminal Equipment is expected to transmit this FEAC code word (to the "Remote" Terminal Equipment), anytime it detects a "Service Affecting" fault condition, within its system.
001110	DS3 LOS (Loss of Signal) Condition	The Terminal Equipment is expected to transmit this FEAC code word (to the "Remote" Terminal Equipment), if it declares a Loss of Signal condition. For more information on the "DS3 LOS Condition", please see Section _.
000000	DS3 OOF (Out of Frame) Condition	The Terminal Equipment is expected to transmit this FEAC code word (to the "Remote" Terminal Equipment), if it declares an OOF Condition. For more information on the "DS3 OOF Condition", please see Section _.
010110	DS3 AIS (Alarm Indication Status) Pattern Received	The Terminal Equipment is expected to transmit this FEAC code word (to the "Remote" Terminal Equipment) if it detects the AIS pattern, in the "incoming" DS3 data stream. For more information on the "DS3 AIS Signal", please see Section _.

Table 1, The Relationship between the FEAC six-bit Code Words and their Meaning (Continued)

FEAC Code Word	Meaning	Comments
011010	DS3 Idle Signal Received	The Terminal Equipment is expected to transmit this FEAC code word (to the "Remote" Terminal Equipment) if it detects the Idle Signal pattern, in the "incoming" DS3 data stream. For more information on the "DS3 Idle Signal", please see Section _
001111	DS3 Equipment Failure - Non Service Effecting	
011101	Common Equipment Failure – Non Service Effecting	
010101	Multiple DS1 LOS	This FEAC Message is only applicable for "Channelized Applications. If the Terminal Equipment detects an LOS, within more than one of its "lower-tributary" DS1 signals, then it (the Terminal Equipment) is expected to do transmit this particular FEAC code word.

Table 1, The Relationship between the FEAC six-bit Code Words and their Meaning (Continued)

FEAC Code Word	Meaning	Comments
000101	DS1 Equipment Failure – Service Affecting	This FEAC Message is only applicable for "Channelized" Applications. If the Terminal Equipment detects a "service affecting" fault condition within the equipment that processes a given "lower tributary" DS1 signal, then it is expected to do the following. 1. Transmit this particular FEAC code word. (The "remote" terminal equipment is interpret this signaling as an indication that one of the equipment, which handles a particular "lower tributary DS1 signal" is experiencing a "service-affecting" fault condition. 2. Transmit the "DS1 Line Number ID" code word, as listed in Table _. (This procedure identifies which "lower tributary" DS1 signal) is experiencing the "service affecting" fault condition

Table 1, The Relationship between the FEAC six-bit Code Words and their Meaning (Continued)

FEAC Code Word	Meaning	Comments
011110	Single DS1 LOS (Loss of Signal) Condition	This FEAC Message is only applicable for "Channelized" Applications. If the Terminal Equipment detects a Loss of Signal condition within one of its "lower tributary" DS1 signals, then it is expected to do the following. 1. Transmit this particular FEAC code word. (The "remote" terminal equipment will interpret this signaling as an indication that one of the "lower tributary DS1" signals is experiencing an LOS condition). 2. Transmit the "DS1 Line Number ID" code word, as listed in Table _. (This procedure identifies which "lower tributary" DS1 signal) is experiencing the LOS condition.

Table 1, The Relationship between the FEAC six-bit Code Words and their Meaning (Continued)

FEAC Code Word	Meaning	Comments
000011	DS1 Equipment Failure – Non-Service Affecting	This FEAC Message is only applicable for "Channelized" Applications. If the Terminal Equipment detects a "non-service" affecting fault condition within the equipment that processes a given "lower tributary" DS1 signal, then it is expected to do the following. 1. Transmit this particular FEAC code word. (The "remote" terminal equipment will interpret this signaling as an indication that one of the equipment, which handles a particular "lower tributary DS1 signal" is experiencing a "non-service affecting" fault condition. 2. Transmit the "DS1 Line Number ID" code word, as listed in Table _. (This procedure identifies which "lower tributary" DS1 signal) is experiencing the "non-service affecting" fault condition.

Table 1, The Relationship between the FEAC six-bit Code Words and their Meaning (Continued)

FEAC Code Word	Meaning	Comments
000111	Line Loop-back Activate	This FEAC Message permits the user to command the "Remote" Terminal Equipment, to configure a "Remote Loop-back" for testing purposes. This command can be used in either "channelized" or "non-channelized" applications. If the Terminal Equipment intends to command the "remote" terminal equipment into a remote loop-back mode, then it should do the following. 1. Transmit this particular FEAC code word. (The "remote" terminal equipment will interpret this signaling as a "loop-back" request). However, the remote terminal equipment still needs to know what kind of loop-back the "local" terminal equipment is requesting. For "channelized" applications, it is possible that the "local" terminal equipment wishes to have a particular DS1 channel (at the remote terminal equipment) to be configured into the "remote" loop-back mode. 2. Transmit the "Line ID Number" FEAC code, as listed in Table _. (This procedure identifies exactly which signal is to be configured into the "remote" loop-back mode.

Table 1, The Relationship between the FEAC six-bit Code Words and their Meaning (Continued)

FEAC Code Word	Meaning	Comments
011100	Line Loop-back Deactivate	This FEAC Message permits the user to command the "Remote Terminal Equipment, to terminate a "Remote Loop-back" configuration. This command can be used in either "channelized" or "non-channelized" applications. If the Terminal Equipment intends to command the "remote" terminal equipment to terminal a remote loop-back mode, then it should do the following. 1. Transmit this particular FEAC code word. (The "remote" terminal equipment will interpret this signaling as a "loop-back" termination request). However, the remote terminal equipment still needs to know what kind of loop-back the "local" terminal equipment wishes to terminate. For "channelized" applications, it is possible that the "local" terminal equipment wishes to have a particular DS1 channel (at the remote terminal equipment) to terminate its "remote" loop-back mode. 2. Transmit the "Line ID Number" FEAC code, as listed in Table _. (This procedure identifies exactly which signal is to terminate is "remote" loop-back mode.

2.2.3 TRANSMITTING AND RECEIVING LAP-D (PMDL) MESSAGES

To be included in the next revision

2.2.4 DETECTION OF "OOF" OUT-OF-FRAME CONDITION

To be included in the next revision

2.2.5 DETECTION OF "LOS" (LOSS OF SIGNAL) CONDITION

To be included in the next revision

2.2.6 DETECTION OF "AIS" (ALARM INDICATION SIGNAL) CONDITION

To be included in the next revision

2.2.7 DETECTION OF THE "IDLE" PATTERN

To be included in the next revision

2.2.8 TRANSMISSION AND RECEPTION OF A FERF (FAR-END-RECEIVE FAILURE)

Each DS3 frame consists of two (2) "X" bits. Each of these bits are set to the exact same value. The "X-bits" within the DS3 framing structure permits a given terminal to transmit a "Yellow Alarm" or "Far-End-Receive Failure" (FERF) to another terminal.

By default, the Transmit DS3 Framer block (within the XRT7250 Framer IC) will transmit a "FERF" or "Yellow Alarm" condition, to the remote terminal equipment, anytime the "Receive DS3 Framer block (also within the same XRT7250 Framer IC) has detected any of the following conditions:

- LOS (Loss of Signal) Condition
- OOF (Out of Frame) Condition
- AIS (Alarm Indication Status) Condition.

Two Examples of How and Why FERF Messages are Transmitted.

Example 1 – Normal Operation

Consider that two DS3 Terminals are communicating with each other and everything is "OK".

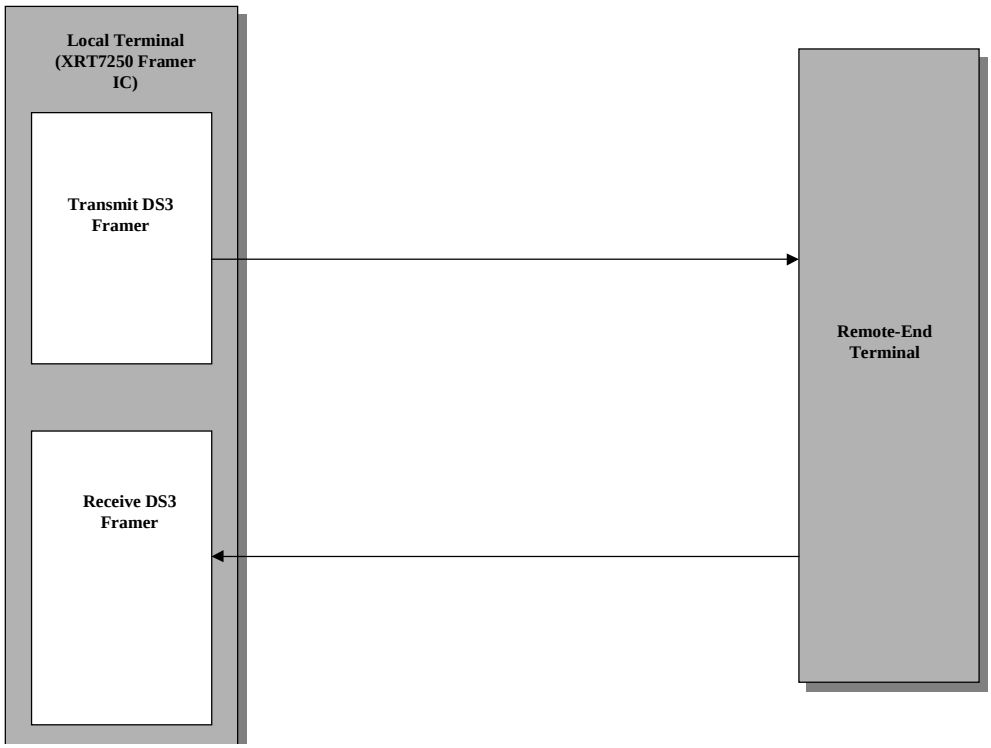


Figure 8, Illustration of two DS3 Terminals communicating with each other, in a "Normal" Manner.

In response to this condition, the Transmit DS3 Framer block (within the "Local" XRT7250 Framer IC) will set the "X" bits (within the very next outbound DS3 frame) to "1", as illustrated below. This form of signaling reflects the "Normal" (e.g., non-Alarm condition).

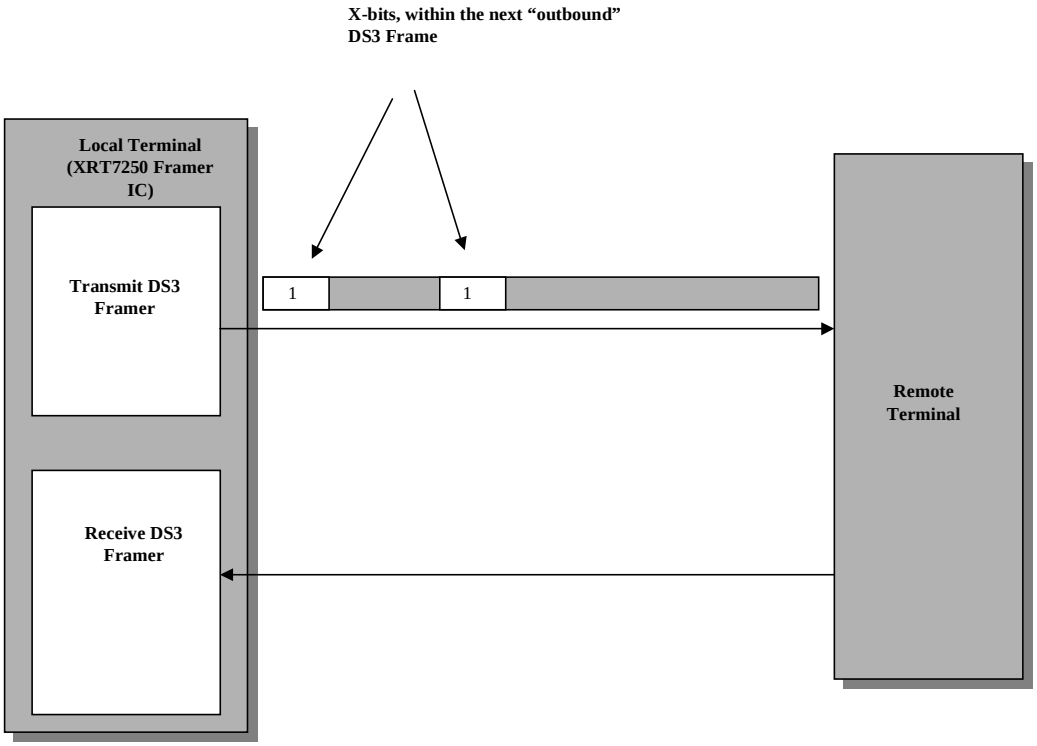


Figure 9, An Illustration of the Local Terminal Transmitting a "Normal" (e.g., non-FERF) Indication to the Remote Terminal Equipment.

Example 2 – Alarm (FERF) Condition

Now, consider that the "Local Terminal Equipment" is declaring an LOS (Loss of Signal) condition, in the signal that it is supposed to be receiving from the "Remote Terminal Equipment".

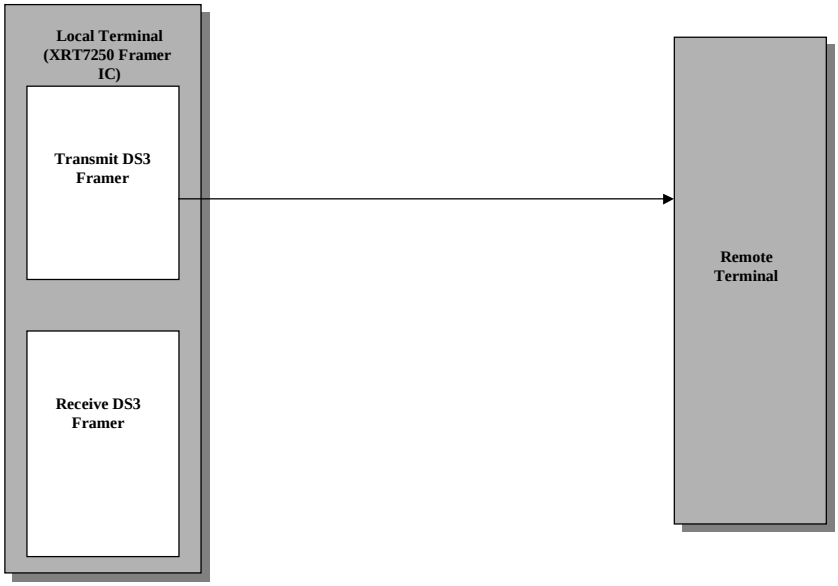


Figure 10, Illustration of the "Local Terminal Equipment" experiencing an "LOS" (Loss of Signal) condition.

In response to this condition, the Transmit DS3 Framer block (within the "Local" XRT7250 Framer IC) will set the "X" bits (within the very next outbound DS3 frame) to "0" as illustrated below. This form of signaling reflects the "FERF" condition.

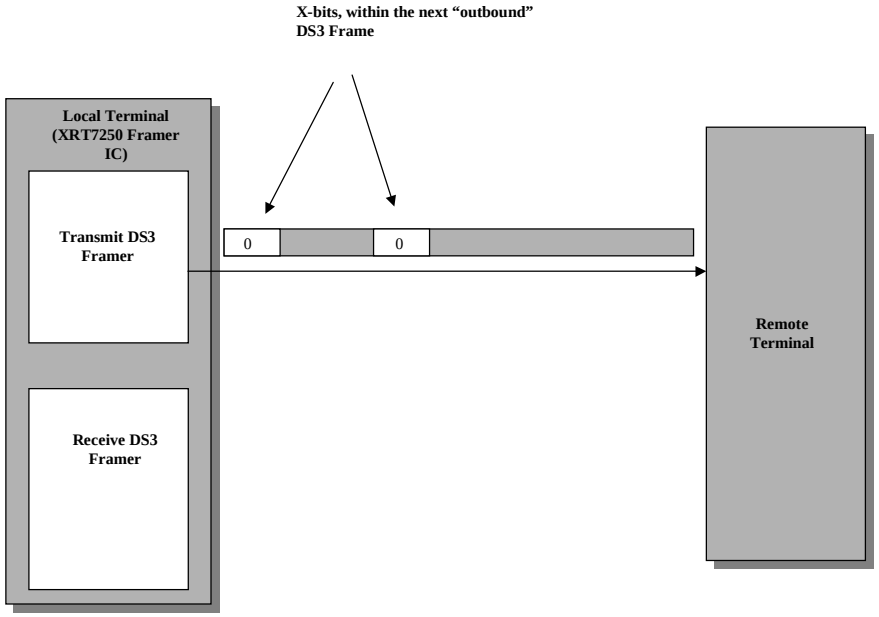


Figure 11, An Illustration of the Local Terminal Transmitting a "FERF" indication to the Remote Terminal Equipment.

NOTE: The "Transmit DS3 Framer" will continue to set the "X" bits to "0" for the duration that the "Receive DS3 Framer" block detects the LOS condition.

2.2.9 TRANSMISSION AND RECEPTION OF A FEBE (FAR-END BLOCK ERROR) INDICATOR.

The “FEBE” (Far-End Block Error) bit-fields, within the DS3 framing structure permits a given terminal to indicate whether or not it is receiving DS3 data (from the Remote Terminal Equipment) in an “Error-Free” manner or not.

The “Local” Terminal Equipment will receive the “inbound” DS3 frames from the “Remote Terminal Equipment”. As the “Local” Terminal Equipment does this, it will also check and verify the P-bits and CP-bits within each “inbound” DS3 frame.

To be completed in the next revision

3. THE RECOMMENDED CONFIGURATION SETTINGS FOR THE XRT7300 LIU IC – FOR DS3 APPLICATIONS

3.1 RECEIVE EQUALIZER SETTING

As mentioned earlier in this Ap Note, the XRT7300 device was designed to be able to receive any "DSX-3" pulse, over any cable length, ranging from 0 to 450 ft; with the Receive Equalizer enabled. As a consequence, the user is advised to enable the "Receive Equalizer" by tying the "REQDIS" input pin (of the XRT7300 device) to GND.

NOTE: For DS3 and STS-1 Applications, the user should only consider disabling the "Receive Equalizer" if he/she intends to use the "Receive Section" (of the XRT7300 device) to monitor the "Transmit Output" of the "Local Terminal Equipment". In this case, the "DS3 line signal" would be "square" in shape (e.g., having a lot of high frequency Fourier components). As a consequence, enabling the "Receive Equalizer" (in this particular case) would result in over-equalization of the pulse and possibly induce bit-errors.

3.2 DECODIS/ENCODIS SETTING

Both the XRT7250 Framer IC and the XRT7300 LIU IC include a "B3ZS Encoder/Decoder" block. In order to prevent the introduction of bit-errors, the user must configure the B3ZS Encoder/Decoders, within these two devices such that:

a. The B3ZS Encoder/Decoder, within the XRT7250 Framer IC is enabled and the B3ZS Encoder/Decoder, within the XRT7300 LIU IC is disabled; or
b. The B3ZS Encoder/Decoder, within the XRT7250 Framer IC is disabled, and the B3ZS Encoder/Decoder, within the XRT7300 LIU IC is enabled.

If the user enables the B3ZS Encoder/Decoders within both the Framer and LIU ICs, then the "outbound" DS3 data will be corrupted and transmitted erroneously.

Of the two above-mentioned choices, the user is advised to select option (a) (e.g., where the B3ZS Encoder/Decoder, within the Framer IC is enabled and that within the LIU IC is disabled). The reason for this recommendation is that this approach permits the user to take advantage of the Performance Monitoring that the Framer IC offers. More specifically, the XRT7250 Framer IC includes the "PMON LCV Event Count Registers";

which is incremented each time the “Receive Section” of the XRT7250 Framer IC detects a Line Code Violation.

If the user were to select the other viable option (e.g., where the B3ZS Encoder/Decoder within the Framer IC is disabled, and that within the LIU IC is enabled); then the user would have to design some glue logic in order to tally the number of Line Code Violations that were detected by the LIU IC.

3.3 LOSTHR SETTING

The user is advised to tie the LOSTHR pin to "HIGH". The rationale for this recommendation follows:

According to the XRT7300 Data Sheet, the relationship between the state of the LOSTHR pin and the resulting "LOS Declaration and Clearance" levels are presented below.

LOSTHR = 0			
Parameter	**Min.**	**Max.**	**Units**
Signal Level to Declare LOS	< 60		mVpk
Signal Level to Clear LOS		> 220	mVpk

LOSTHR = 1			
Parameter	**Min.**	**Max.**	**Units**
Signal Level to Declare LOS	< 25		mVpk
Signal Level to Clear LOS		> 90	mVpk

According to the various Bellcore and ANSI specifications, the DS3 line signal (at the DSX-3 Cross-Connect) can range in amplitude between 360mVpk and 850mVpk. Now, the Receive Function of a DS3 LIU must be able to receive a line signal which has been attenuated by an additional 450 feet (beyond the DSX-3 Cross-Connect). This additional 450 feet of cable, results in an additional attenuation (of the line signal) by approximately 6dB. Hence, a signal which was of amplitude 360mVpk at the DSX-3, will be at approximately 180mVpk at the Receiving Terminal.

If the signal level (at this Receiving Terminal) were ever to drop below 60mV, then the XRT7300 device would declare an LOS condition. However, in order for the XRT7300 device to "clear" the LOS defect, then the signal level must rise above 220mVpk. According to the above-mentioned scenario, the signal level will never rise above 180mVpk. Hence, the LIU will never clear LOS.

Setting the LOSTHR pin to "HIGH" permits the XRT7300 device to properly detect and clear the LOS Defect.

4. THE RECOMMENDED CONFIGURATION SETTINGS FOR THE XRT7250 FRAMER IC – FOR DS3 APPLICATIONS

4.1 TxLineClk Invert Selection

The XRT7250 Framer IC permits the user to configure the "Transmit Section" of the device to output its "Single-Rail" or "Dual-Rail" data, via the "TxPOS" and "TxNEG" output pins (to the LIU IC) on either the rising edge or the falling edge of the "TxLineClk" signal. The purpose of this feature is to ensure that the Framer IC can always be configured to output this data (to the LIU IC) without violating any "set-up" or "hold-times".

Figure 12 presents an illustration of the behavior of the "TxPOS" and "TxNEG" output pins, when the XRT7250 Framer IC is configured to output this data upon the rising edge of "TxLineClk".

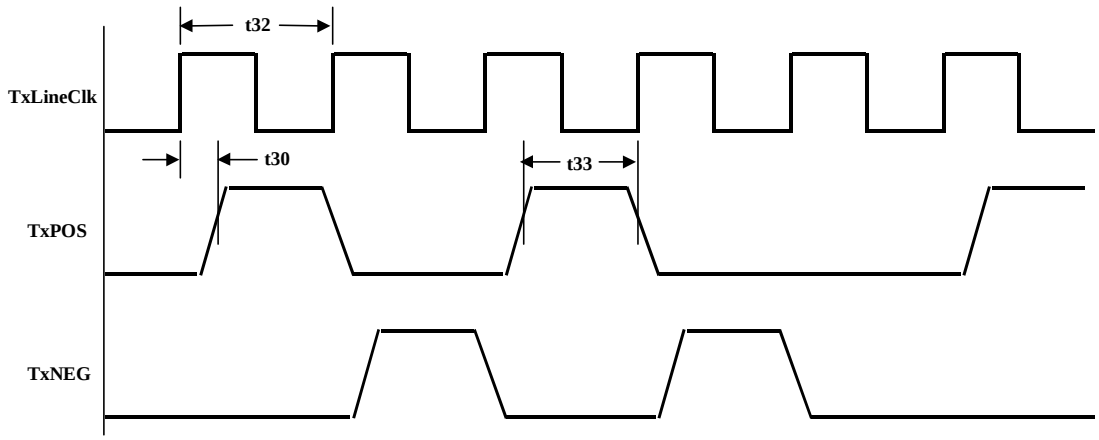


Figure 12, An Illustration of the Behavior of the "TxPOS" and "TxNEG" output signals, when the XRT7250 Framer IC is configured to output data on the rising edge of "TxLineClk".

Likewise, Figure 13 presents an illustration of the behavior of the "TxPOS" and "TxNEG" output pins, when the XRT7250 Framer IC is configured to output this data upon the falling edge of "TxLineClk".

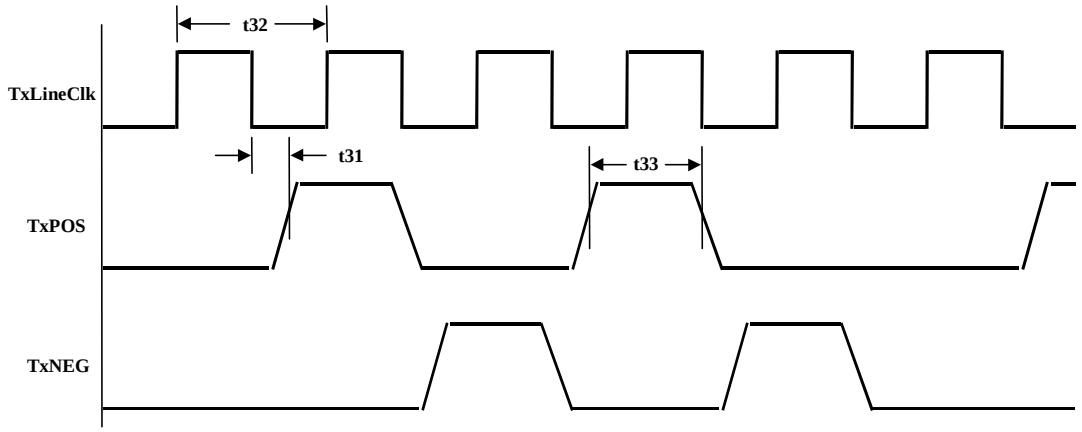


Figure 13, An Illustration of the Behavior of the "TxPOS" and "TxNEG" output signals, when the XRT7250 Framer IC is configured to output data on the falling edge of "TxLineClk".

The user can configure the XRT7250 Framer IC into either of these modes by writing the appropriate value into the "TxLineClk Invert" bit-field, within the "I/O Control" Register (Address Location: 0x01, within the Framer IC Address space).

I/O Control Register (Address = 0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Setting this bit-field to “0” configures the XRT7250 device to output data, via the TxPOS and TxNEG output pins, on the “rising” edge of “TxLineClk”. Conversely, setting this bit-field to “1” configures the XRT7250 device to output data, via the “TxPOS” and “TxNEG” output pins, on the falling edge of “TxLineClk”.

How does the XRT7300 LIU handle this transmit data?

In order to decide whether to configure the Framer IC to output its “TxPOS” and “TxNEG” data upon either the rising or falling edge of “TxLineClk” it is important to know the following.

- Which clock edge (of “TxLineClk”) does the XRT7300 LIU IC use to sample the “TxPOS” and “TxNEG” data?
- What are the “set-up” and “hold” time requirements, of the XRT7300 device, around this clock edge.
- What are the “TxLineClk” to “TxPOS” and “TxNEG” output delays of the Framer IC?

Figure 14 illustrates how the XRT7300 LIU IC samples the “TxPOS” and “TxNEG” data (from the Framer IC).

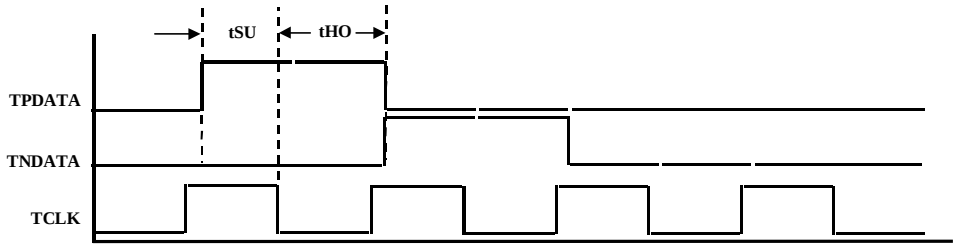


Figure 14, Illustration of how the "Transmit Input" of the XRT7300 LIU IC samples the data on its "TPDATA (or TxPOS)" and "TNDATA (or TxNEG)" input pins.

Figure 14 indicates that the XRT7300 device samples the both the "TxPOS" (or TPDATA) and the "TxNEG" (or TNDATA) upon the falling edge of the "TxLineClk" (or TCLK) clock signal.

Figures 12, 13, and 14 all present waveforms of the "Transmit Output Clock" and "Data" (from the XRT7250 Framer IC), which is to be sampled by the XRT7300 LIU IC. These figures all include timing parameter numbers which are tabulated below.

Table 2, Listing of Relevant Timing Parameters, for Interfacing the "Transmit LIU Interface" block (within the XRT7250 Framer IC) to the Transmit Section of the LIU IC

Name	Description	Min.	Typ.	Max.	Units
t30	Rising edge of "TxLineClk" to "TxPOS" and "TxNEG" output delay from the XRT7250 Framer IC (When "TxPOS" and "TxNEG" are configured to be output upon rising edge of "TxLineClk". (See Figure _).	0.7		2.0	ns
t31	Falling edge of "TxLineClk" to "TxPOS" and "TxNEG" output delay from the XRT7250 Framer IC (When "TxPOS" and "TxNEG" are configured to be output upon the falling edge of "TxLineClk" (See Figure _).	0.7		1.5	ns
tSU	"TxPOS" and "TxNEG" data to falling edge of "TxLineClk" set-up time requirement of the XRT7300 LIU IC.	3			ns
tHO	"TxPOS" and "TxNEG" data hold time requirement (for the XRT7300 LIU IC), from the falling edge of "TxLineClk"	3			ns

Conclusion:

Based upon all of this information, it is best to configure the XRT7250 Framer IC to output its "TxPOS" and "TxNEG" data (to the XRT7300 LIU IC) upon the rising edge of "TxLineClk". This configuration permits the XRT7300 device to sample the "TxPOS" and "TxNEG" data near the middle of the bit-period. Hence, the user is advised to set the "TxLineClk Invert" bit-field (within the "I/O Control" Register) to "0", as depicted below.

I/O Control Register (Address = 0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	X	0

4.2 RxLineClk Invert Selection

The XRT7250 Framer IC permits the user to configure the "Receive Section" of the device to sample the "incoming Single-Rail" or "Dual-Rail" data, (from the XRT7300 LIU IC) via either rising edge or the falling edge of the "RxLineClk" signal. The purpose of this feature is to ensure that the Framer IC can always be configured to sample this data (from the LIU IC) without violating any "set-up" or "hold-times".

Figure 15 presents an illustration of how the XRT7250 Framer IC samples the "incoming" data (from the LIU IC) via the "RxPOS" and "RxNEG" input pins, when it (the XRT7250 Framer IC) is configured to sample this data on the rising edge of the "RxLineClk" signal.

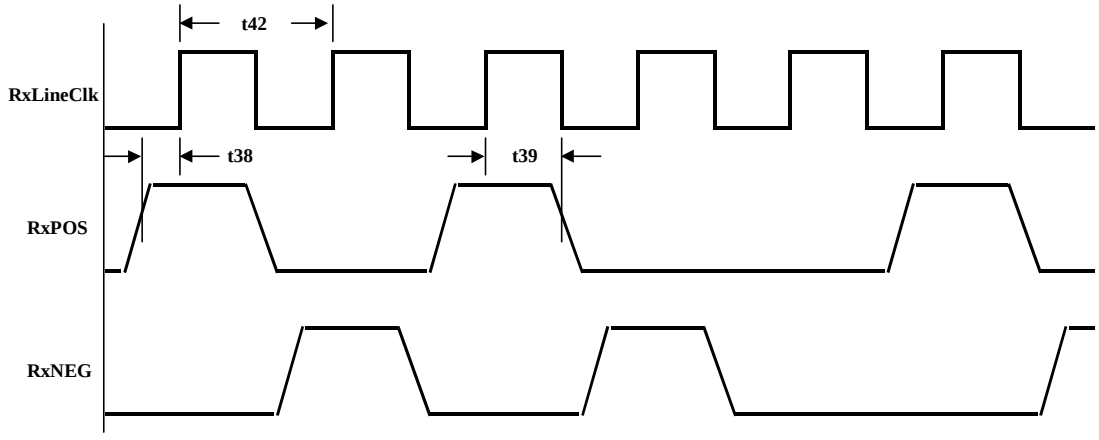


Figure 15, An Illustration of How the XRT7250 Framer IC samples the "incoming" data (from the LIU IC) via the "RxPOS" and "RxNEG" input pins, when it is configured to sample this data on the rising edge of the "RxLineClk" signal.

Likewise, Figure 16 presents an illustration of how the XRT7250 Framer IC samples the "incoming" data (from the LIU IC) via the "RxPOS" and "RxNEG" input pins, when it (the XRT7250 Framer IC) is configured to sample this data on the falling edge of the "RxLineClk" signal.

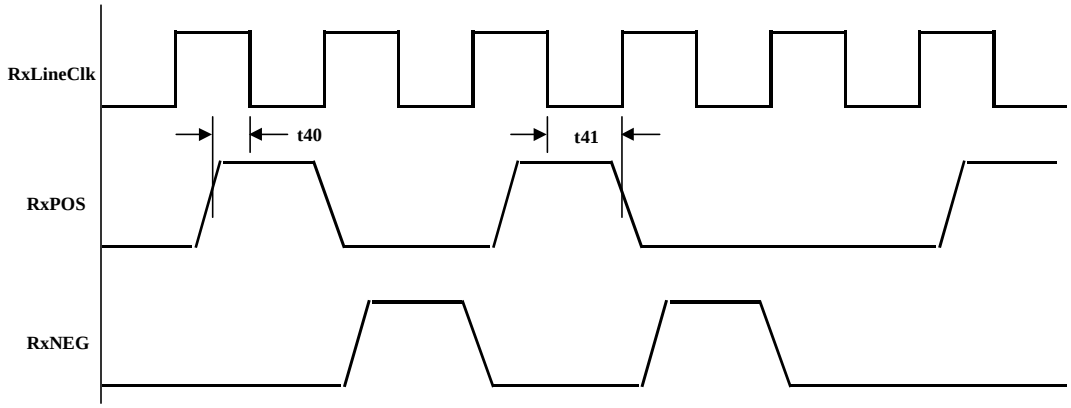


Figure 16, An Illustration of How the XRT7250 Framer IC samples the "incoming" data (from the LIU IC) via the "RxPOS" and "RxNEG" input pins, when it is configured to sample this data on the falling edge of the "RxLineClk" signal.

The user can configure the XRT7250 Framer IC into either of these modes by writing the appropriate value into the "RxLineClk Invert" bit-field, within the "I/O Control" Register (Address Location: 0x01, within the Framer IC Address space).

I/O Control Register (Address = 0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	0	0

Setting this bit-field to "0" configures the XRT7250 device to latch the data on the "RxPOS" and "RxNEG" input pins, into the device, on the "rising" edge of "RxLineClk". Conversely, setting this bit-field to "1" configures the XRT7250 device to latch the data on the RxPOS and RxNEG input pins, into the device, data, on the falling edge of RxLineClk.

How does the XRT7300 LIU IC output this "receive data" to the Framer IC?

In order to decide whether to configure the Framer IC to sample the "RxPOS" and "RxNEG" data upon either the rising or falling edge of "RxLineClk" it is important to know the following.

- Which clock edge (of "RxLineClk") does the XRT7300 LIU IC) output its "Receive Data" via the "RxPOS" (RPOS) and "RxNEG" (RNEG) output pins?
- What are the "set-up" and "hold" time requirements, of the XRT7250 device, around this clock edge?
- What are the "RxLineClk" to "RPOS" and "RNEG" output delays of the LIU IC?

Figure 17 illustrates the behavior of the "RxLineClk", "RxPOS", and "RxNEG" signals (from the XRT7300 LIU IC) as it outputs this recovered data and clock to the Framer IC.

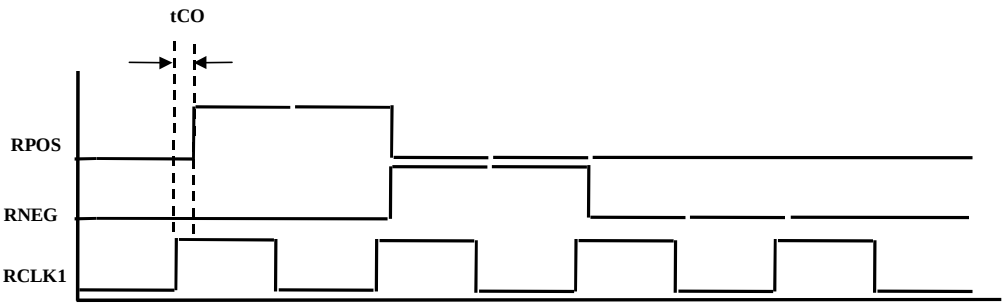


Figure 17, Illustration of the behavior of the "RxPOS" (RPOS), "RxNEG" (RNEG) output and "RxLineClk" (RCLK1) output signals from the XRT7300 LIU IC.

Figure 17 indicates that the XRT7300 device outputs its "recovered" data (via the "RPOS" and "RNEG" output pins) upon the rising edge of the "RCLK1" (or "RxLineClk) clock signal.

Figures 15, 16, and 17 all present waveforms of the "Receive Output Clock" and "Data" (from the XRT7300 LIU IC) which is to be sampled by the XRT7250 Framer IC. These figures all include timing parameter numbers which are tabulated below.

Table 3, Listing of Relevant Timing Parameters, for Interfacing the "Receive LIU Interface" block (within the XRT7250 Framer IC) to the Receive Section of the LIU IC

Name	Description	Min.	Typ.	Max.	Units
t38	"RxPOS" and "RxNEG" to the rising edge of "RxLineClk" set-up time requirement for the XRT7250 Framer IC. (When "RxPOS" and "RxNEG" are configured to be sampled upon the rising edge of "RxLineClk" (See Figure _).	10			ns
t39	"RxPOS" and "RxNEG" data to the "rising edge of "RxLineClk" hold-time requirements of the Framer IC (When "RxPOS" and "RxNEG" are configured to be sampled upon the rising edge of "RxLineClk" (See Figure _).	5			ns
t40	"RxPOS" and "RxNEG" to the falling edge of "RxLineClk" set-up time requirement for the XRT7250 Framer IC. (When "RxPOS" and "RxNEG" are configured to be sampled upon the falling edge of "RxLineClk" (See Figure _).	10			
t41	"RxPOS" and "RxNEG" data to the "falling edge of "RxLineClk" hold-time requirements of the Framer IC (When "RxPOS" and "RxNEG" are configured to be sampled upon the falling edge of "RxLineClk" (See Figure _).	5			
tCO	Rising edge of "RCLK" to "RxPOS" and "RxNEG" output delay of the XRT7300 LIU IC	0		4	ns

Conclusion:

Based upon all of this information, it is best to configure the XRT7250 Framer IC to sample the "RxPOS" and "RxNEG" data (from the XRT7300 LIU IC) upon the falling edge of "RxLineClk". This configuration permits the XRT7250 device to sample the "RxPOS" and "RxNEG" data near the middle of the bit-period. Hence, the user is

advised to set the "RxLineClk Invert" bit-field (within the "I/O Control" Register) to "1", as depicted below.

I/O Control Register (Address = 0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable TxLOC	LOC	Disable RxLOC	AMI/ ZeroSup*	Unipolar/ Bipolar*	TxLine Clk Invert	RxLine Clk Invert	Reframe
R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	0	0	1	0

4.3 Timing Reference/Framing Selection

To be provided in the next revision

4.4 B3ZS Encoder/Decoder Setting

The user is advised to (1) enable the "B3ZS Encoder/Decoder", within the Framer IC and to disable the "B3ZS Encoder/Decoder" within the LIU IC. The reason for this recommendation is two-fold:

a. To insure that bit-errors (due to "over-encoding") are not induced in the "Transmit Output" data; (e.g., if the "B3ZS Encoder/Decoder blocks" within both the Framer and LIU are enabled) and
b. To permit the user to take advantage of the "Performance Monitoring" features within the Framer IC. In particular, the Framer contains the "PMON LCV Event Count" Registers (located at Address = 0x50 and 0x51).

5. INTERFACING THE XRT7250 DS3/E3 FRAMER TO THE XRT7300 DS3/E3/STS-1 LIU IC CONSIDERATION

Figure 18 presents a schematic drawing of a possible approach to interfacing the XRT7250 Framer IC to the XRT7300 LIU device for DS3 Applications, only. It should be noted that this schematic would not be appropriate for Line Card designs that are intended to:

- To support only E3 applications; or
- To be configurable in order to support either DS3 or E3 applications.

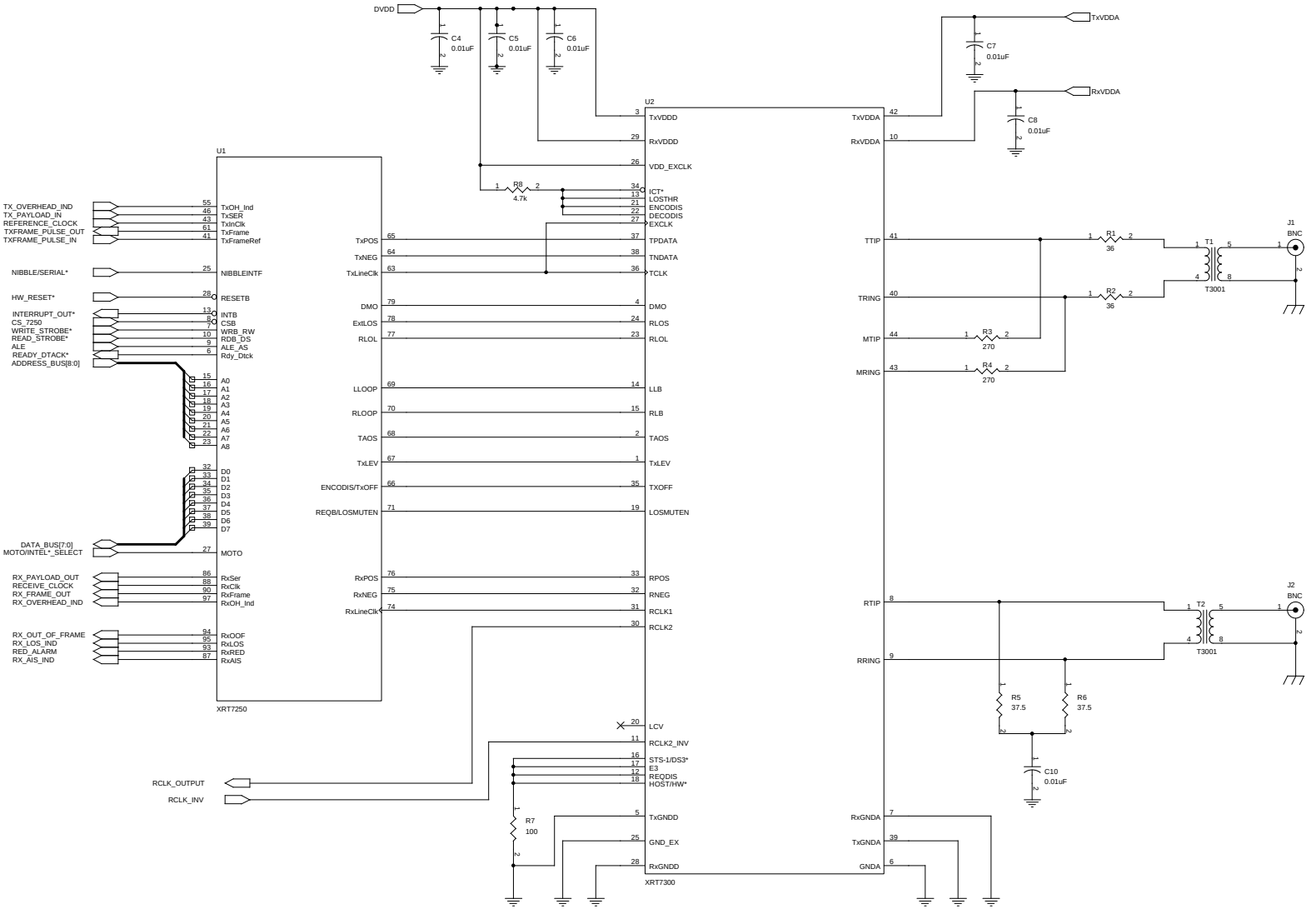
The reason for this is as follows.

a. The Receive Equalizer enable/disable input pin (of the LIU IC) to pulled to GND; thereby enabling the Receive Equalizer (within the LIU) for all conditions.
b. The "Transmit Line Build-Out" input pin (TxLEV) is wired to a general purpose output of the XRT7250 Framer IC. This permits the user to either enable or disable the "Transmit Line Build-Out" circuit (within the LIU) in order to meet the Isolated Pulse Template (per Bellcore GR-499-CORE) at the Digital Cross Connect (DSX-3) location.

There are numerous other things that the user should notice about this schematic.

a. The XRT7300 LIU IC is configured to operate in the "Hardware" Mode. In the "Hardware" Mode, all configuration settings, for the LIU IC, are controlled via the various input pins.
b. The following input pins (to the LIU IC) are connected to some general purpose output pins of XRT7250 Framer IC.
   - TxLEV – The "Transmit Line Build-Out" circuit enable/disable control pin.
   - LOSMUTEN – The "MUTing-upon-LOS" mode enable/disable control pin.
   - LLB – The "Local Loop-back" enable/disable control pin
   - RLB – The "Remote Loop-back" enable/disable control pin
   - TxOFF – The "Transmit Shut-OFF" control pin
   - TAOS – The "Transmit All Ones" control pin
c. The "EXCLK" (External Reference Clock) input pin of the XRT7300 LIU IC is driven by the "TxLineClk" (Transmit Line Clock) signal from the Framer IC. This same signal is (of course) used to drive the "TCLK" input pin of the XRT7300 LIU IC.

   NOTE: This setting is not appropriate if the user intends to operate their line card in the "loop-timed" mode (e.g., where the "Transmit Clock" signal, for both the Framer and LIU ICs are derived from the "Recovered Line Clock" signal, "RCLK" or



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"RxLineClk"). Figure 19 presents a recommended schematic for "Loop-Timing" Applications.

d. The "ENCODIS" and "DECODIS" input pins are pulled up to VDD. This setting disables both the "B3ZS Encoder" and "B3ZS Decoder" blocks within the LIU IC.

NOTE: This setting requises that the user enable the "B3ZS Encoder and Decoder" within the XRT7250 Framer IC.

e. The XRT7250 Framer IC is connected to the XRT7300 LIU IC, in a "Dual-Rail" Manner.

NOTE: This is required, if the "B3ZS Encoder and Decoder" blocks, within the XRT7250 Framer IC is to enabled.

f. The RLOS, RLOL and DMO Output pins (from the LIU IC) are wired to some general purpose input pins of the XRT7250 Framer IC.

5.1 CONTROLLING THE XRT7300 VIA THE LINE INTERFACE DRIVE REGISTER (WITHIN THE XRT7250 FRAMER IC)

To be provided in the next revision

5.2 TRANSMIT LINE BUILD-OUT SETTING

To be provided in the next revision

5.3 MUTING UPON LOS

To be provided in the next revision

5.4 REMOTE AND LOCAL LOOP-BACKS

The combination of the XRT7250 Framer IC and the XRT7300 LIU IC supports the following loop-back modes.

- Framer Local Loop-back Mode
- LIU – Analog Local Loop-back Mode
- LIU – Digital Local Loop-back Mode
- LIU – Remote Loop-back Mode.

Each of these "Loop-back" Modes will be briefly described below.

5.4.1 Framer Local Loop-back Mode

The XRT7250 Framer IC supports the "Framer Local Loop-back" Mode. Figure 20 illustrates the data path, when this loop-back mode is selected.

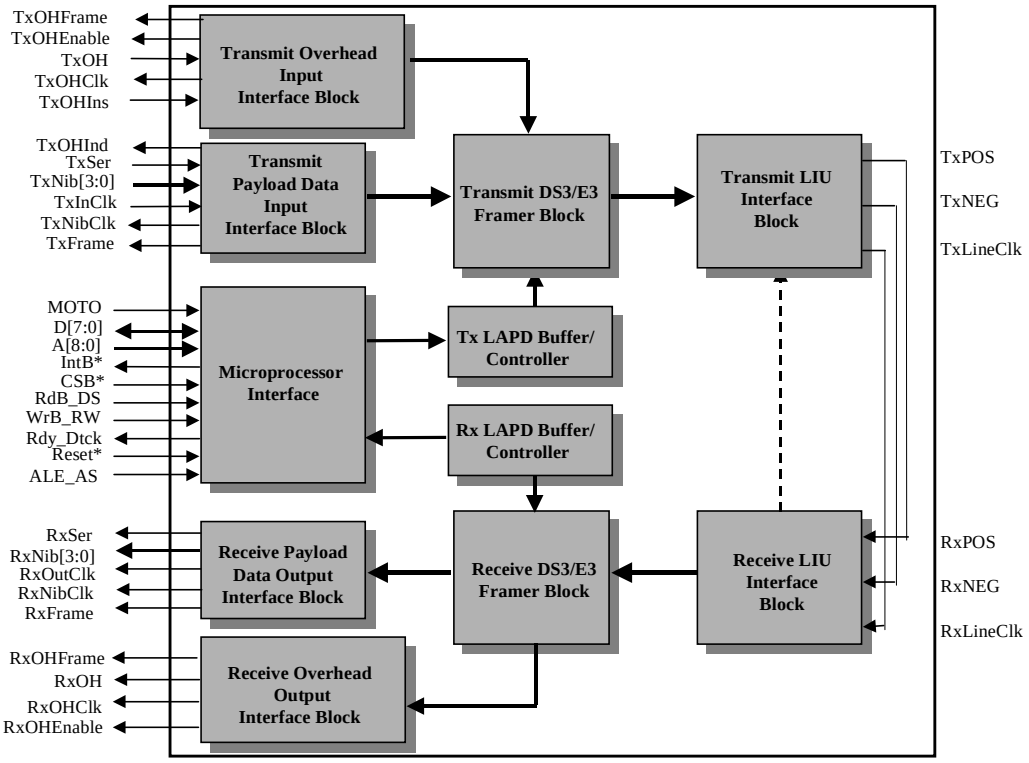

Figure 20, Illustration of the Data Path, when the XRT7250 Framer IC is configured to operate in the Local Loop-back Mode.

When the XRT7250 Framer IC is configured to operate in the "Local Loop-back" Mode, then the "TxPOS", "TxNEG", and "TxLineClk" output signals, will be (internally) looped back into the "RxPOS", "RxNEG", and "RxLineClk" input signals.

The user can configure the XRT7250 Framer IC to operate in the Local Loop-back Mode by setting the "Local Loop-back" bit-field (within the "Framer Operating Mode" Register) to "1", as illustrated below.

Framer Operating Mode Register (Address = 0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Local Loopback	DS3/ E3*	Internal LOS Enable	RESET	Interrupt Enable Reset	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	1

NOTE: If the user configures the Framer IC to operate in the "Local Loop-back" Mode, then it is imperative that the user NOT configure the XRT7250 Framer IC into the "Loop-Timing" Mode. In other words, the user must insure that the "TimRefSel[1:0]" bit-fields are not assigned the values "[0, 0]".

5.4.2 LIU – Analog Local Loop-back Mode

The XRT7300 DS3/E3/STS-1 LIU IC supports the "Analog Local Loop-back" Mode. This particular loop-back mode is very much an "end-to-end" loop-back mode (within the LIU IC) as illustrated below in Figure 21.

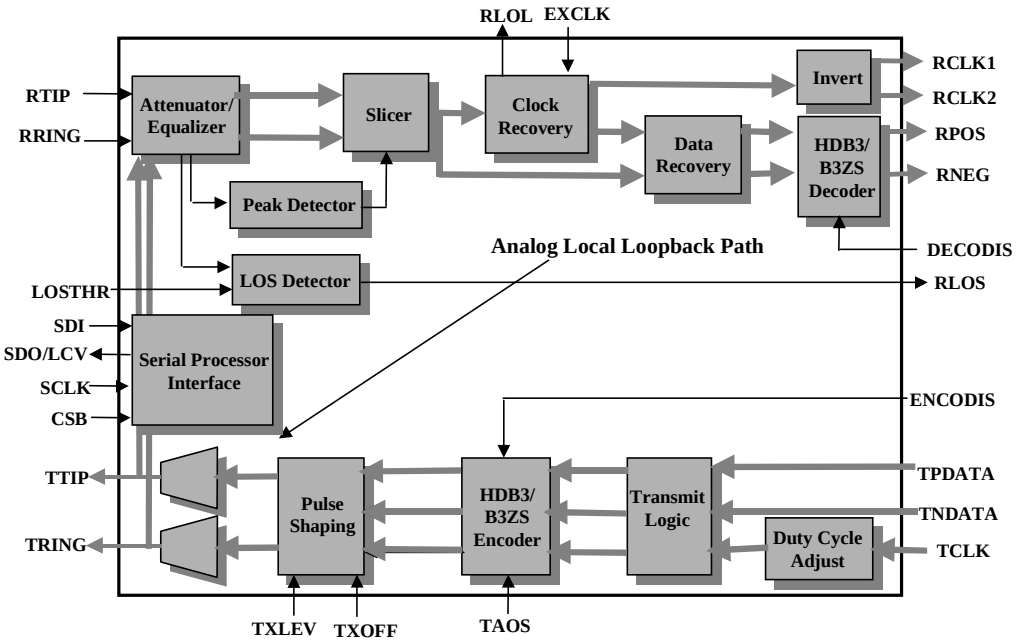

Figure 21, An Illustration of the "LIU – Analog Local Loop-back" Mode

When the XRT7300 LIU IC is operating in the "Analog Local Loop-back" Mode, the data path will proceed through the entire "Transmit Section" (e.g., from the "TPDATA", "TNDATA" and TCLK" inputs all the way to the line output (e.g., "TTIP" and "TRING"). In fact this signal is also output onto the line and is transmitted to the "Remote Terminal Equipment". In parallel, this "Transmit" Data (located at the "TTIP" and "TRING" pads) is internally routed over the "Receive Section" of the XRT7300 device. From this point on, the data will proceed through the remainder of the "Receive Section" (within the device) all the way out to the "RPOS", "RNEG" and "RCLK" output pins.

Application Note – Considerations for Designing the XRT7250 and XRT7300 Device in a DS3 Line Card Application (Preliminary)

Rev. 1.00

April 7, 2000

How to configure the XRT7300 device into the "Analog Local Loop-back" Mode.
Whenever the XRT7300 LIU IC is operating in the "Hardware" Mode, then it can be configured to operate in the "Analog Local Loop-back" Mode, by setting the "LLB" input pin to "HIGH" and setting the "RLB" input pin to "LOW". If the XRT7250 Framer IC is interfaced to the XRT7300 LIU IC, in the manner as illustrated in Figure _, then the user simply writes the value "xxxx xx01" into the "Line Interface Drive" Register (located at Address 0x80, within the XRT7250 Framer IC), as illustrated below.

Line Interface Drive Register (Address = 0x80)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		REQB **(LOSMUTEN)**	**TAOS**	Encodis **(TxOFF)**	**TxLEV**	**RLOOP**	**LLOOP**
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	X	1	X	0	1

NOTE: The "Bold" Type, in the "Line Interface Drive" Register bit-format reflects the role that these bit-fields plays, when interfaced to the XRT7300 LIU IC, as shown in Figure 18.

SUBTLE THINGS THAT ONE SHOULD KNOW ABOUT THE ANALOG LOCAL LOOP-BACK MODE
When designing a DS3 Line Card, the user should bear the following things in mind, if he/she intends to configure the XRT7300 LIU IC into the "Analog Local Loop-back" Mode.

1. Whatever data is input into the XRT7300 device, via the "TPDATA" and "TNDATA" input pins will also be output on the line, via the "TTIP" and "TRING" output pins.
2. The "Analog Local Loop-back" Mode will not function if the user invokes the "TxOFF" feature. This is because the "TxOFF" feature disables the Transmit Output drivers, which resides within the "Analog Local Loop-back Mode" data path.

NOTE: This aspect of the "Analog Local Loop-back" Mode can be undesirable in those applications where "System Redundancy" is required. For "System Redundancy" Applications, the user is advised to use the "Digital Local Loop-back" Mode instead.

3. Anytime the XRT7300 device is configured to operate in the "Analog Local Loop-back" Mode, it (the LIU IC) will automatically declare an LOS (Loss of Signal) condition. Hence, the "Analog Local Loop-back" feature will not function if the "MUTing-upon-LOS" feature is enabled.

NOTE: In the "Analog Local Loop-back" Mode, the XRT7300 device will declare an LOS condition, independent of whether there is a DS3 line at the RTIP and RRING input pins or not.

5.4.3 LIU – Digital Local Loop-back Mode

The XRT7300 DS3/E3/STS-1 LIU IC supports the "Digital Local Loop-back" Mode. This particular loop-back mode is not as much an "end-to-end" loop-back mode (within the LIU IC) as is the "Analog Local Loop-back" Mode. A simple illustration of the "Digital Local Loop-back" Mode is presented in Figure 22.

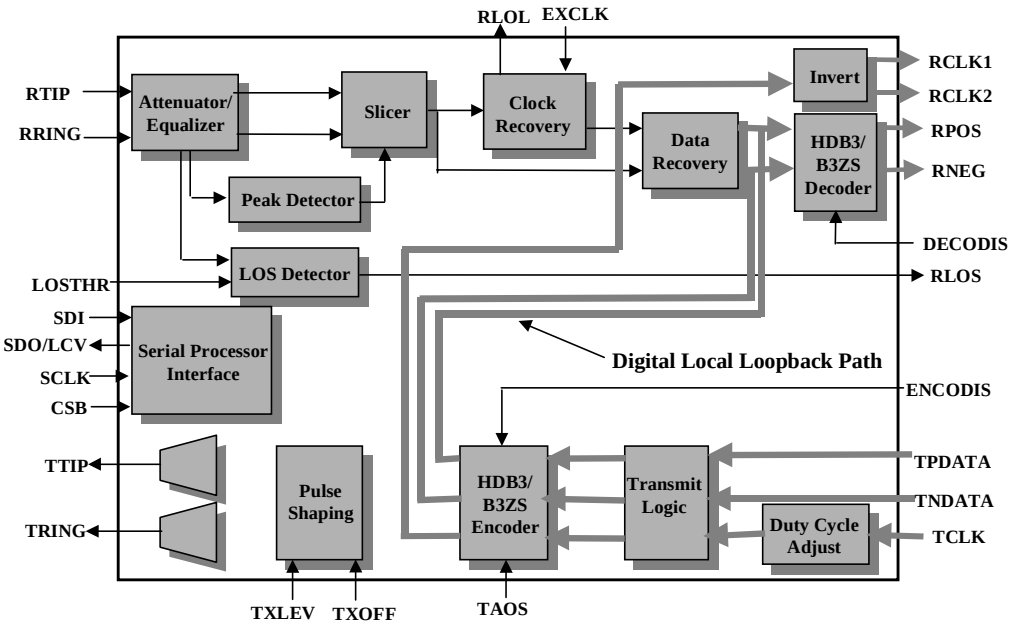

Figure 22, An Illustration of the "LIU – Digital Local Loop-back" Mode

When the XRT7300 LIU IC is operating in the "Digital Local Loop-back" Mode, the data path will proceed through the entire "Transmit Section" (e.g., from the "TPDATA", "TNDATA" and "TCLK" inputs all the way to the line output (e.g., the "TTIP" and "TRING"). In fact this signal is also output onto the line and is transmitted to the "Remote Terminal Equipment". In parallel, this "Transmit" Data (located at the output of the "HDB3/B3ZS Encoder" block) is looped back into the input of the "HDB3/B3ZS

Decoder" block (within the "Receive Path). From this point on, the data will proceed through the remainder of the "Receive Section (within the device) all the way out to the "RPOS", "RNEG", and "RCLK" output pins.

How to configure the XRT7300 device into the "Digital Local Loop-back" Mode.
Whenever the XRT7300 LIU IC is operating in the "Hardware" Mode, then it can be configured to operate in the "Digital Local Loop-back" Mode, by setting both the "LLB" and "RLB" input pins to "HIGH". If the XRT7250 Framer IC is interfaced to the XRT7300 LIU IC, in the manner as illustrated in Figure _, then the user simply writes the value "xxxx xx11" into the "Line Interface Drive" Register (located at Address 0x80, within the XRT7250 Framer IC), as illustrated below.

Line Interface Drive Register (Address = 0x80)

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
		REQB **(LOSMUTEN)**	**TAOS**	Encodis **(TxOFF)**	**TxLEV**	**RLOOP**	**LLOOP**
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	X	1	X	1	1

NOTE: The "Bold" Type, in the "Line Interface Drive" Register bit-format reflects the role that these bit-fields plays, when interfaced to the XRT7300 LIU IC, as shown in Figure 18.

SUBTLE THINGS THAT ONE SHOULD KNOW ABOUT THE DIGITAL LOCAL LOOP-BACK MODE
When designing a DS3 Line Card, the user should bear the following things in mind, if he/she intends to configures the XRT7300 LIU IC into the "Digital Local Loop-back" Mode.

1. Whatever data is input into the XRT7300 device, via the "TPDATA" and "TNDATA" input pins will also be output on the line, via the "TTIP" and "TRING" output pins.
2. The "Digital Local Loop-back" Mode WILL function if the user invokes the "TxOFF" feature. This is because the "Transmit Output driver" (which is disabled by the "TxOFF" feature) does not reside within the "Digital Local Loop-back Mode" data path.

NOTE: This aspect of the "Digital Local Loop-back" Mode is very useful in those applications where "System Redundancy" is required.

3. The XRT7300 device declares and clears LOS (Loss of Signal) normally, whenever it is operating in the "Digital Local Loop-back" Mode. Hence, if a DS3 line signal is

presents at the "RTIP" and "RRING" input pins, then the XRT7300 device will NOT declares an LOS condition. Conversely, if no DS3 line signal is present at the "RTIP" and "RRING" input pins, then the XRT7300 device will declare an LOS condition.

5.4.4 LIU – Remote Loop-back Mode

The XRT7300 DS3/E3/STS-1 LIU IC supports the "Remote Loop-back" Mode. Figure 23 presents an illustration as to how this particular loop-back mode functions.

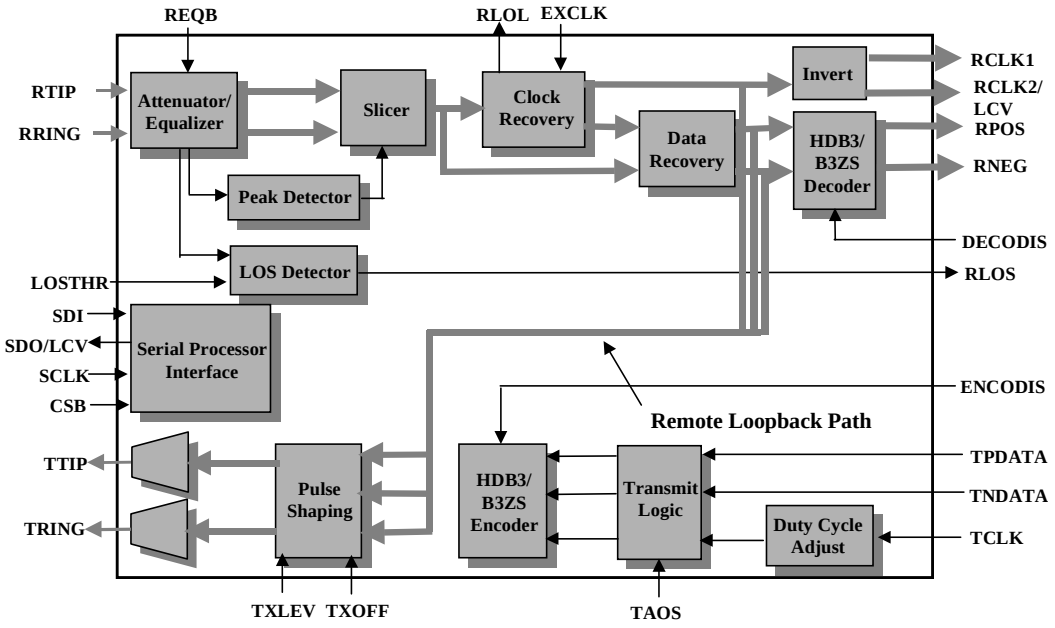

Figure 23, An Illustration of the "LIU – Remote Local Loop-back" Mode.

When the XRT7300 LIU IC is operating in the "Remote Loop-back" Mode, the data path will originate from the "Remote Terminal Equipment" and will proceed through the entire "Receive Section" of the XRT7300 LIU IC. In fact, this "incoming" data will be output to the "Terminal Equipment" via the "RPOS" and "RNEG" output pins. In parallel, this "Receive" Data (located at the input of the "HDB3/B3ZS Decoder" block) is looped back into the input of the "Pulse-Shaping" circuitry within the "Transmit Section"

of the LIU IC. From this point on, the data will proceed through the remainder of the "Transmit Section" (within the LIU IC), and will be output onto the line (back towards the "Remote Terminal Equipment") via the "TTIP" and "TRING" output pins.

How to configure the XRT7300 device into the "Remote Loop-back" Mode.
Whenever the XRT7300 LIU IC is operating in the "Hardware" Mode, then it can be configured to operate in the "Remote Loop-back" Mode, by setting the "RLB" input pin to "HIGH" and the "LLB" input pin to "LOW". If the XRT7250 Framer IC is interfaced to the XRT7300 LIU IC, in the manner as illustrated in Figure _, then the user simply writes the value "xxxx xx10" into the "Line Interface Drive" Register (located at Address 0x80, within the XRT7250 Framer IC), as illustrated below.

Line Interface Drive Register (Address = 0x80)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		REQB **(LOSMUTEN)**	**TAOS**	Encodis **(TxOFF)**	**TxLEV**	**RLOOP**	**LLOOP**
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	X	1	X	1	0

NOTE: The "Bold" Type, in the "Line Interface Drive" Register bit-format reflects the role that these bit-fields plays, when interfaced to the XRT7300 LIU IC, as shown in Figure 18.

SUBTLE THINGS THAT ONE SHOULD KNOW ABOUT THE REMOTE LOCAL LOOP-BACK MODE
When designing a DS3 Line Card, the user should bear the following things in mind, if he/she intends to configure the XRT7300 LIU IC into the "Remote Local Loop-back" Mode.

1. The XRT7300 LIU IC will perform data and clock recovery on all data that is received via the "RTIP" and "RRING" input pins. This data and clock signals will be output (to the "Local Terminal Equipment") via the "RPOS", "RNEG" and RCLK output pins.
2. The user must insure that the source of the clock (applied to the "EXCLK" input pin) is not derived from the "incoming" line signal. Hence, the user must source the "EXCLK" input pin with a local timing source.

5.5 TAOS (TRANSMIT ALL ONES) PATTERN

To be included in the Next Revision

5.6 TXOFF FEATURE

The XRT7300 LIU IC permits the user to turn on or off the "Transmit Output Driver" via the "TxOFF" feature. If this feature is invoked, then the "TTIP" and "TRING" output pins (to the line) will be tri-stated. If this feature is disabled, and if a clock signal is applied to the TCLK input pin (of the XRT7300 device), then the XRT7300 device will output data via the "TTIP" and "TRING" output pins, based upon data that is sampled on the "TPDATA" and "TNDATA" input pins.

The "TxOFF" feature is a useful feature under the following conditions.

1. In systems that will employ "system redundancy" considerations.

NOTE: A more detailed discussion of how the "TxOFF" feature is useful in "System Redundancy" design is presented in Section _.

2. In those applications, where the user wishes to insure that "random" data is not output on the line, upon "DS3 Line Card" insertion and power up.

6. MONITORING THE XRT7300 VIA THE LINE INTERFACE SCAN REGISTER (WITHIN THE XRT7250 FRAMER IC)

To be included in the next revision

6.1 CHECKING FOR LOS

To be included in the next revision

6.2 CHECKING FOR DMO

To be included in the next revision

6.3 CHECKING FOR RLOL

To be included in the next revision

7. DIAGNOSTIC TESTING

To be included in the next revison

7.1 LIU - REMOTE LOOP-BACK TESTING

To be included in the next revision

7.2 LIU - ANALOG LOCAL LOOP-BACK TESTING

To be included in the next revision

7.3 LIU - DIGITAL LOCAL LOOP-BACK TESTING

To be included in the next revision

7.4 FRAMER – LOCAL LOOP-BACK TESTING

To be included in the next revision

8. SYSTEM REDUNDANCY DESIGN CONSIDERATIONS

To be included in the next revision

9. IDENTIFICATION OF FRAMING FORMAT OF "INCOMING" DS3 DATA STREAM.

To be included in the next revision

10. SOFTWARE/FIRMWARE DESIGN CONSIDERATIONS

10.1 INITIALIZATION ROUTINES

To be included in the next revision

10.2 INTERRUPT SERVICE ROUTINES

To be included in the next revision